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Flux/underfill Compatibility Study for Flip-chip Assembly Process

Phuthanate Phoosekieaw[1+] and Sanya Khunkhao[1]

[1]Faculty of Engineering, Department of Electrical Engineering
Sripatum University, 61 Phaholyothin Rd, Jatujak, Bangkok 10900, Tel (662) 579-1111 Ext: 2272

Abstract. The rapid uptake of flip-chip technology within the electronics industry due to their better thermal performance, smaller size, lower profile, light weight, and higher input/output density, the solder joints together with underfill in flip chip package serve as a mechanical mechanism for resisting the thermal deformation induced by the coefficient of thermal expansion (CTE) mismatch between silicon die and substrate. underfill materials are employed in flip-chip assemblies to enhance solder joint reliability performance. The adhesion of underfills with solders is important to the integrity of the flip-chip structure. The effect of temperature and humidity aging as well as flux residue on adhesion strength was also investigated.

Keywords: Flip chip, Underfill, Tacky flux

1. Introduction

Electronics manufacturers are investigating new lead-free alloys and their effects on the reflow process. once lead-free processes are well developed, determining the effect of these changes on the various materials sets used in electronic assemblies is important. The leading lead-free alloy candidates are the different tin-silver-copper (Sn/Ag/Cu) formulations. The Sn/Ag/Cu eutectic system has a melting point of 217°C significantly higher than the 183°C melting point of eutectic tin/lead (Sn/Pb) alloy. These new alloys increase the peak reflow temperature from 220°C up to 240 or 260°C, a factor that affects material performance. This study deals with one aspect of lead-free processing for flip chip in a package. Flipchip underfill adhesion to lead-free flux residues, The interaction between the flux and the underfill is important for the long-term reliability of underfilled flip chip devices. All fluxes leave behind residues after reflow. When properly processed, no-clean or low-solid flux residues do not degrade electrical performance but will affect the adhesion and flow of the underfill. Elevated lead-free processing temperatures change the characteristics of the flux residues after reflow. This study examines tacky fluxes for their ability to provide a reliable and consistent interconnect in a lead-free flip chip reflow process. After initial evaluation, parts were conditioned, and reliability was assessed to determine JEDEC level 3 with a 260°C reflow compatibility. The 260°C peak reflow temperature simulates the worst possible reflow conditions that a package can undergo in a surface-mount manufacturing process. Parts were then evaluated using scanning acoustic microscopy [4] for evidence that the flux residues affected reliability. Flux residues can affect reliability in two different ways. Present on the solder bump, substrate or die, thin films of flux residue can significantly reduce interfacial adhesion between the flux and the surfaces. Once the underfilled device is stressed by thermal shock, humidity or other factors, the underfill delaminates from the surface, and a gap can be detected using acoustic microscopy. Fluxes can also affect reliability by physically impeding the flow of underfill material. Flux residue buildup in the gap between bumps or between the die and the substrate can narrow the gap to a point where the underfill cannot flow or the edges flow faster, encapsulating air and creating a void. To ensure a void-free underfill, homogenous wetting of the underfill must occur on all surfaces. If wetting is not homogenous, voids in the uncured underfill may translate into reliability problems later. With the change to a lead-free reflow process, the characteristics of the flux residues change significantly.

+ Corresponding author. Tel.: + (6629636401); fax: +(6629636409).
E-mail address: (phuthanate@svi.co.th).

2. Preparation and Experimental Procedure

2.1. Assembly

The test component was a GNRU07-003LF IC GNR FLIPCHIP NP4* with polyimide passivation. Two lead-free alloys were used as bump metallurgy [1]: Sn/3.5 Ag/0.5 Cu and Sn/3.0 Ag/1.0 Cu. The substrate was a four-layer BT laminate at a thickness of 1mm. The solder mask was PSR4000 AUS5, and the surface finish on the pads was electroless nickel/immersion gold (ENIG). The assembly was performed using the following procedure. The flip chips were dipped into a Thin film flux pot with a dip/coating height set to 50 microns and placed using an UNIVERSAL GENESIS GI-14D The parts were then reflowed using a SEATRONICS RF-820-N under nitrogen (less than 200 ppm) using a lead-free profile with a peak temp of 245°C. After reflow, the devices were underfilled with either of two underfills [Table 1] using a CAMALOT 1818 automated dispenser. Both underfills were treated to the same cure cycle [3]: ramp to 165°C over one hour, then held at 165°C for one hour. [Figure1,2,3,4]

Table 1: Underfill systems used in lead-free flux evaluation

Property	UF A	UF B
Curative	Anhydride	Anhydride
Filler	60% (silica)	64% (silica)
CTE [[alpha].sub.1	44	22
[T.sub.9]	140	120

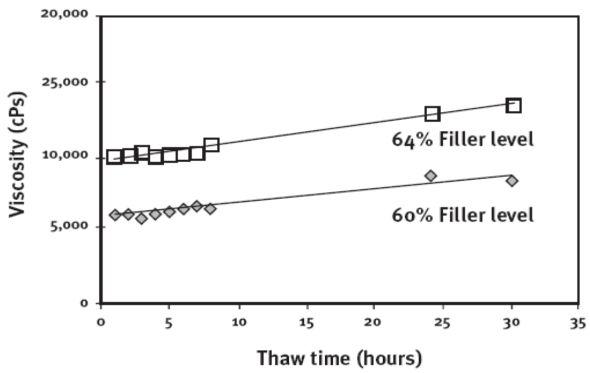

Fig. 1: underfill viscosity

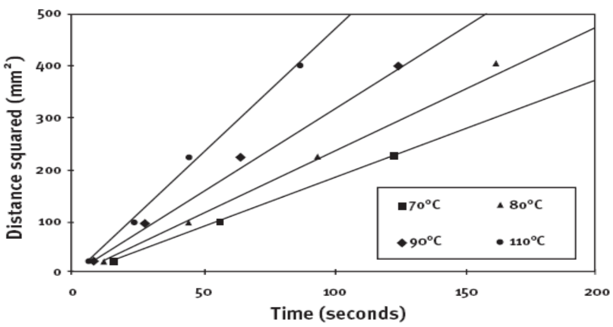

Fig. 2: process windows for the underfill flow

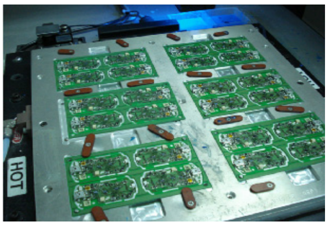

Fig. 3: underfill process

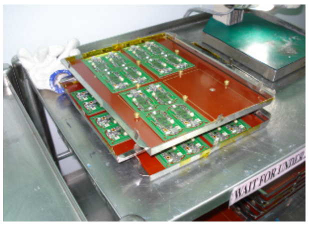

Fig. 4: cure cycle

2.2. Testing Setup

After curing, a SONIX C-SAM®D-9000 C-MODE scanning acoustic microscope imaged all parts using a 110 MHz w/8mm focus. At this point, some parts were set aside for cross-sectioning to measure the die to substrate gap. After recording the initial acoustic images, the parts were conditioned as per JEDEC level 3 testing [Table 2]. Parts were baked at 125°C for 24 hours to establish the same moisture level baseline for all parts, then conditioned for 192 hours at 30°C/60% relative humidity (RH), as per the J-STD-022. After conditioning, the parts were subjected to three lead-free reflows with a peak temperature of 260°C and imaged again using the acoustic microscope. [Figure 5,6,7]

Table 2: JEDEC pre-conditioning environment as per J-STD 022A

Level	Time	Conditions
1	168	85°C / 85% RH
2	168	85°C / 60% RH
2a	696	30°C / 60% RH
3	192	30°C / 60% RH
4	96	30°C / 60% RH
5	72	30°C / 60% RH
5a	48	30°C / 60% RH
6	TOL	30°C / 60% RH

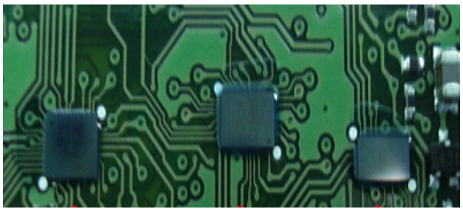

Fig. 5: Flip chip underfill

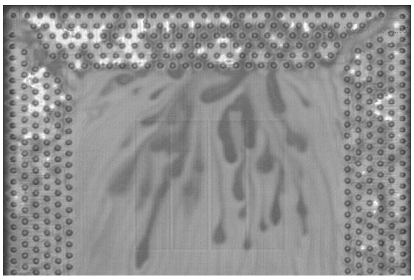

Fig.6: Flip chip underfill voids

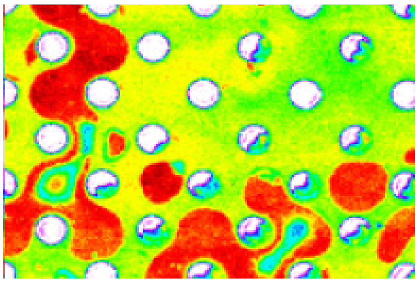

Fig. 7: voids in the underfill (red)

2.3. Result and Discussion

A. Initial Wetting

Wetting and gap height were measured on select samples. When the flux system worked properly, the solder bump melted and wetted out along the pad, the package collapsed, and the overall gap height was reduced. Based on gap heights, fluxes were designated with performances of good, fair or failure. Failures correspond to a lack of connection between the flip chip and the substrate pads. A summary of the results is presented in [Table 3].

Table 3: Initial solder joint evaluation

Flux	RUN 1		RUN 2		RUN 3	
	Underfill Gap (um)	Joint Quality	Underfill Gap (um)	Joint Quality	Underfill Gap (um)	Joint Quality
A	-	-	-	-	60	Good
B	70	Good	77	Good	63	Good
C	73	Good	83	Good	64	Good
D	-	-	91	Excess Flow	-	-
E	-	-	83	Good	60	Good
F	77	Fair	102	No Connection	108	No Connection
G	76	Fair	81	Good	62	Good
H	66	-	81	Good	-	-
I	86	Good	-	-	-	-
J	-	Poor	83	Good	63	Good
K	-	-	-	-	65	Good
L	-	-	80	-	63	Good
M	-	-	81	Good	65	Good
N	-	-	83	Good	64	Good
O	-	-	83	Good	-	-
P	-	-	-	-	61	Good
Q	77	Fair	84	Good	-	-

Solder joints were evaluated over three separate builds. Since slight variations occurred in the solder mask definition, the gap heights were only comparable within a column. Other criteria used to evaluate soldering performance were wetting to the pad, bump shape after collapse and overall solder joint appearance. Most fluxes met the requirements of lead-free reflow of flip chips in a nitrogen environment.

B. JEDEC Level 3/260°C Reliability

This study used JEDEC testing to determine flux residue/underfill compatibility. With flux residue compatibility, moisture conditioning [2] and subsequent thermal treatment can force a failure when moisture intrudes where the underfill does not adhere well to the flux residue.

Table 4 : summary of flux / underfill performance

Flux	Joint Quality	performance with UF A	performance with UF B	overall performance

A	Good	Good	Fair	UF A only
B	Good	Poor	Good	UF B only
C	Good	Poor	Good	UF B only
D	Poor	Poor	Poor	Poor
E	Good	Fair	Good	UF B only
F	Good	Good	Good	Excellent
G	Good	Poor	Poor	Poor
H	Good	Poor	Poor	UF B only
I	Good	Poor	Good	UF B only
J	Good	Poor	Good	UF B only
K	Good	Poor	Good	UF B only
L	Good	Good	Good	Excellent
M	Good	Poor	Good	UF B only
N	Good	Good	Good	Excellent
O	Good	Poor	Good	UF B only
P	Good	Good	Good	Excellent
Q	Good	Fair	Good	UF B only

As flux residues may be slightly hygroscopic, any moisture that does penetrate an exposed flux surface can be absorbed. This condition is exacerbated when poor adhesion occurs between the underfill and the flux residues. After exposure to moisture conditioning, the parts were reflowed three times with a peak temp of 260°C. During reflow, any absorbed moisture within the part expands (popcorn crack), creating the voids observed in the acoustic microscopy images. A summary of all the flux/underfill systems examined and their performance are presented in [Table 4]. Out of all the fluxes examined, only two were incompatible with both underfill systems. Four fluxes exhibited excellent performance characteristics with both underfills. Most of the fluxes were compatible only with underfill System B. One proprietary epoxy flux system showed better performance with underfill A over underfill B.

2.4. Conclusions

The movement to a lead-free process affects the moisture level rating of packages and devices. One of the materials that impacts this JEDEC moisture level rating is the underfill. This study shows that some flux residue/underfill systems are suitable for lead-free processes. Flux Systems G, L, N, and P are more compatible to different underfill material sets than others. underfill System B, developed with a chemistry specifically designed to interact with flux residues and meet JEDEC level 3/260°C requirements, shows excellent compatibility with almost all the flux residues.

3. Acknowledgements

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