2011 International Conference on Information and Electronics Engineering
IPCSIT vol.6 (2011) © (2011) IACSIT Press, Singapore

Process Induced Random Variation Models of Nanoscale MOS Performance: Efficient tool for the nanoscale regime analog/mixed signal CMOS statistical/variability aware design

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Abstract. In this research, the novel models of random variation in I_{ds} which is a key parameter of any MOS transistor, have been proposed in this research as the probability density functions. Both triode and saturation regions have been explored. Unlike the previous researches, this research has been performed based upon the up to dated nanoscale regime MOS equations. The proposed models for both regions have been verified at 65 nm technology by using the Monte Carlo simulation and the Kolmogorov-Smirnof goodness of fit test (KS-test). These models are very accurate since they can fit the Monte Carlo based distribution with 99% confidence. Hence, the proposed models have been found to be efficient for the statistical/variability aware design of various CMOS analog/mixed signal circuits and systems in the nanoscale regime.

Keywords: Nanoscale, CMOS, analog, mixed signal, statistical design, variability aware design

1. Introduction

Process induced random variations in MOS transistor level parameters play a very important role in the statistical/variability aware design of CMOS analog/mixed signal circuits and systems. These variations produce the random mismatches in MOS performances which are reflected as random variations in circuit level parameters for example, Ids, gm, gmb and rds etc. Obviously, Ids has been found to be the key parameter since it is the basis for the derivations of the others. For the MOS transistor level parameters, one of the major variations is that in the threshold voltage which is traditionally modeled as a normally distributed random variable with zero mean where as many models have been proposed for the variance for example [1], [2], [3] and [4] etc.

For the analysis/design simplicity, random variations in MOS circuit level parameters have been explored and modeled as proposed in many previous researches for example [5] and [6] etc. In [6], the percentage of variations in Ids and related circuit level parameters have been modeled as the function of the percentage of variation in threshold voltage. However, the model derivation basis adopted in [6] rely on the simple sensitivity analysis which only the standard deviations of the threshold voltage and the modeled parameters have been mentioned, where as the corresponding actual distribution functions have not been discussed. Furthermore, these previous researches have been performed based upon the conventional MOS equations which are invalid in the nanoscale regime.

Hence, the novel models of random variation in Ids which is a key parameter as mentioned above have been proposed in this research as the complete probability density functions not the standard deviations. Obviously, means, variance, moments and other statistical parameters can be determined by using the proposed model. Both triode and saturation regions have been explored. Unlike the previous researches, this research has been performed based upon the up to dated nanoscale regime MOS equations. The proposed models for both regions have been verified at 65 nm technology by using the Monte Carlo simulation and the Kolmogorov-Smirnof goodness of fit test (KS-test). These models are very accurate since they can fit the Monte Carlo based distribution with 99% confidence according to the KS-test results. Hence, the proposed

models have been found to be efficience for the statistical/variability aware design of various CMOS analog/mixed signal circuits and systems in the nanoscale regime.

2. The Proposed Models

In this section, the proposed models for both triode and saturation regions will be discussed respectively. Before proceed further, it should be mentioned here that the Pelgrom's model for the variation in threshold voltage which has been proposed in [1] is adopted for this research since it is the most often cited. At the nanoscale regime, the devices are closely spaced. Hence, the probability density function of the random threshold voltage variation (ΔV_t) can be given by

$$f_{\Delta Vt}(\delta V_t) = \frac{1}{\sqrt{2\pi}} \frac{WL}{A_{V_t}^2} \exp\left[-\frac{WL\,\delta V_t^2}{2A_{V_t}^2} \right] \tag{1}$$

where A_{Vt} , δV_t , W and L denote the proportional constant of random threshold voltage variation, any sampled value of ΔV_t , channel width and channel length respectively.

In the upcoming subsection, the proposed model for the triode region will be discussed.

2.1. Triode region model

In the ideal situation which process induced random variation can be neglected, I_{ds} of the nanoscale transistor operated in the triode region of operation can be given by

$$I_{ds(ideal)} = WC_{ox}\left[\frac{2(V_{gs} - V_t)V_{ds} - V_{ds}^2}{V_{ds} + \mu^{-1}Lv_{sat}} \right] v_{sat} \tag{2}$$

where C_{ox}, μ and v_{sat} denote gate oxide capacitance, device mobility and saturation velocity respectively. Of course, the above $I_{ds(ideal)}$ is a deterministic variable.

Including the effect of ΔV_t which is a random variable as stated earlier, I_{ds} becomes a random variable which can be given as follows

$$I_{ds} = WC_{ox}\left[\frac{2[V_{gs} - (V_t + \Delta V_t)]V_{ds} - V_{ds}^2}{V_{ds} + \mu^{-1}Lv_{sat}} \right] v_{sat} \tag{3}$$

So, the resulting random variation in I_{ds} which denoted by ΔI_{ds} can be simply determined from (2) and (3) as a simple linear function of ΔV_t as follows

$$\Delta I_{ds} = \left[-\frac{2WC_{ox}V_{ds}v_{sat}}{V_{ds} + \mu^{-1}Lv_{sat}} \right] \Delta V_t \tag{4}$$

Obviously, ΔI_{ds} is a random variable and its probability density functions which is our proposed model for the triode region of operation can be simply given by

$$\begin{aligned} f_{\Delta I_{ds}}(\delta I_{ds}) = {} & \frac{(V_{ds} + \mu^{-1}Lv_{sat})WL}{4\sqrt{2\pi}\,A_{Vt}^2 WC_{ox}V_{ds}v_{sat}} \\ & \times \exp\left[-\frac{(V_{ds} + \mu^{-1}Lv_{sat})WL\delta I_{ds}^2}{16A_{Vt}^2 WC_{ox}V_{ds}v_{sat}} \right] \end{aligned} \tag{5}$$

At this point, mean of ΔI_{DS} can be evaluated as follows

$$\overline{\Delta I_{ds}} = \int_{-\infty}^{\infty} \delta I_{ds} f_{\Delta I_{ds}}(\delta I_{ds})\, d\delta I_{ds} = 0 \tag{6}$$

And the corresponding variance can be given by

$$\sigma^2_{\Delta I_{ds}} = \int_{-\infty}^{\infty} (\delta I_{ds} - \mu_{\Delta I_{ds}})^2 f_{\Delta Ids}(\delta I_{ds}) d\delta I_{ds} = \frac{4A_{Vt}^2 WC_{ox} V_{ds} v_{sat}}{(V_{ds} + \mu^{-1} L v_{sat}) WL} \tag{7}$$

In the next subsection, the proposed model for the saturation region of operation will be introduced.

2.2. Saturation region model

In the ideal situation, I_{ds} of the nanoscale transistor operates in the saturation region is a deterministic variable which can be given by

$$I_{ds(ideal)} = WC_{ox}(V_{gs} - V_t) v_{sat} \tag{8}$$

Including the effect of ΔV_t, I_{ds} becomes a random variable and can be given as follows

$$I_{ds} = WC_{ox}[V_{gs} - (V_t + \Delta V_t)] v_{sat} \tag{9}$$

So, the resulting ΔI_{ds} can be simply determined from (8) and (9) as follows

$$\Delta I_{ds} = -WC_{ox} v_{sat} \Delta V_t \tag{10}$$

As a function of ΔV_t, ΔI_{ds} is a random variable and its probability density functions which is our proposed model for the saturation region of operation can be simply given by

$$f_{\Delta I_{ds}}(\delta I_{ds}) = \frac{WL}{\sqrt{2\pi}(WC_{ox} v_{sat} A_{Vt})^2} \times \exp\left[-\frac{WL \delta I_{ds}^2}{2(WC_{ox} v_{sat} A_{Vt})^2} \right] \tag{11}$$

So, mean of ΔI_{ds} can be evaluated as follows

$$\overline{\Delta I_{ds}} = \int_{-\infty}^{\infty} \delta I_{ds} f_{\Delta I_{ds}}(\delta I_{ds}) d\delta I_{ds} = 0 \tag{12}$$

And the corresponding variance can be given by

$$\sigma^2_{\Delta I_{ds}} = \int_{-\infty}^{\infty} (\delta I_{ds} - \mu_{\Delta I_{ds}})^2 f_{\Delta Ids}(\delta I_{ds}) d\delta I_{ds} = \frac{(WC_{ox} v_{sat} A_{Vt})^2}{WL} \tag{13}$$

Before leaving this section, since the KS-test which relies on the cumulative distribution function has been adopted in this research, it is worthy to evaluate the proposed models in their cumulative distribution function forms. For the triode region, the proposed model in its cumulative distribution function form ($F_{\Delta I_{ds}}(\delta I_{ds})$) can be found by using (5) as follows

$$F_{\Delta I_{ds}}(\delta I_{ds}) = \int_{-\infty}^{\delta I_{ds}} f_{\Delta I_{ds}}(u)du = \frac{1}{2}\left\{1 + erf\left[\frac{\sqrt{(V_{ds} + \mu^{-1}Lv_{sat})WL}\,\delta I_{ds}}{A_{Vt}\sqrt{8WC_{ox}V_{ds}v_{sat}}}\right]\right\} \quad (14)$$

For the saturation region, $F_{\Delta I_{ds}}(\delta I_{ds})$ can be obtained by using (11) as follows

$$F_{\Delta I_{ds}}(\delta I_{ds}) = \int_{-\infty}^{\delta I_{ds}} f_{\Delta I_{ds}}(u)du = \frac{1}{2}\left\{1 + erf\left[\frac{\sqrt{WL}\,\delta I_{DS}}{\sqrt{2}A_{Vt}WC_{ox}v_{sat}}\right]\right\} \quad (15)$$

where $erf(x)$ denotes the error function of any arbitrary variable, x which can be mathematically defined as $erf(x) = \frac{2}{\sqrt{\pi}}\int_0^x \exp(-u^2)du$.

3. The Verification

The verifications of the proposed models have been performed in both qualitative and quantitative aspects. In the qualitative aspects, the estimated probability density functions of ΔI_{ds} obtained from both models have been graphically compared to their actual counterparts obtained from the Monte Carlo simulation of test circuits.

On the other hand for the quantitative aspects, the KS-tests have been performed by using the similar data to that adopted in the qualitative verification. According to [7], KS-test can be performed by the comparison of the K-S test statistic (KS) and the critical value (c). Any model can fit its target data set if and only if its KS is not larger than its c [7].

According to [7], KS can be defined for this research as

$$KS = \max_{\delta I_{ds}}\left\{\left|F_{\Delta I_{ds}}(\delta I_{ds})\big|_{actual}\right| - \left|F_{\Delta Ids}(\delta I_{ds})\big|_{\mathrm{mod}\,el}\right|\right\} \quad (16)$$

where $F_{\Delta I_{ds}}(\delta I_{ds})\big|_{\mathrm{mod}\,el}$ and $F_{\Delta I_{ds}}(\delta I_{ds})\big|_{actual}$ denote the cumulative distribution function forms of the estimated probability density functions obtained from the proposed models and the actual cumulative distribution functions obtained from the test circuits respectively.

On the other hand, as the confidence level of the test is 99% or $\alpha = 0.01$ in the other words, c can be given by [8]

$$c = \frac{1.63}{\sqrt{n}} \quad (17)$$

where n denotes the number of samples.

Before proceed to the verifications, it should be mentioned here that the verifications of the proposed models for both regions have been performed based upon the CMOS technology at 65 nm level by using n = 150 which yields c = 0.133089. In the upcoming subsection, the verification of the model for the triode region will be discussed.

3.1. Triode region model verification

For the verification of the triode region model, a single MOS transistor active resistor at 65 nm technology has been adopted as the test circuit. This circuit is depicted in Fig.1 where $R(V_{gs})$ denotes its resulting resistance which can be elctronically controlled via V_{gs}. Of course, $R(V_{gs})$ can be simply given by

$$R(V_{gs}) = \frac{Lv_{sat}}{2\mu WC_{ox}(V_{gs} - V_t)} \tag{18}$$

The obtained graphical comparison of the probability density functions which is the qualitative model verification as stated above, is depicted in Fig. 2. It can be seen that a strong agreement between the estimated and actual probability density functions can be observed. Hence, proposed triode region model has been graphically verified as highly accurate.

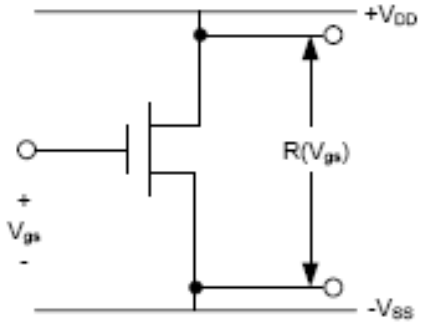

Fig.1: Test circuit for triode region model verification: a single MOS active resistor

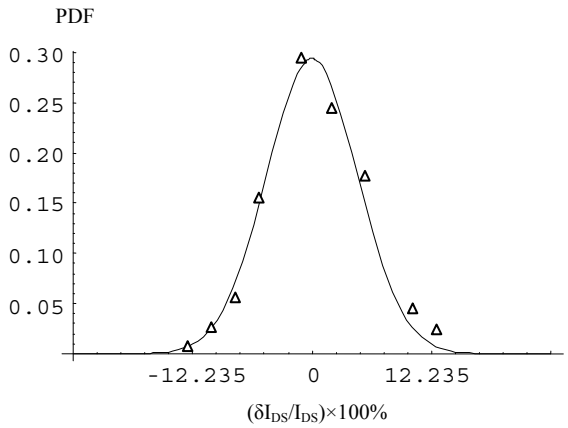

Fig.2: Triode region PDF Comparison: estimated PDF from the model (line), actual PDF from the test circuit (Δ).

For the quantitative verification, it can be seen that the resulting KS can be found from (16) as KS = 0.13306 which is smaller than c = 0.133089. This means that the proposed triode region model can fit the ΔI_{ds} obtained from the test circuit with 99% confidence. At this point, the triode region model is also quantitatively verified as highly accurate.

3.2. Saturation region model verification

On the other hand, for the case of the saturation region model, a diode connected 65 nm MOS transistor has been chosen as the test circuit and can be depicted in Fig.3. The similar graphical comparison of the probability density functions is depicted in Fig. 4. In this case, a strong agreement between the estimated and actual probability density functions can also be observed. Hence, proposed saturation region model has been qualitatively verified as highly accurate.

For the verification in the quantitative aspect, the resulting KS can be found as KS = 0.115654 which is smaller than c = 0.133089. This means that the proposed saturation region model can also fit the ΔI_{ds} obtained from the test circuit with 99% confidence. Hence, the saturation region model has also been quantitatively verified as highly accurate.

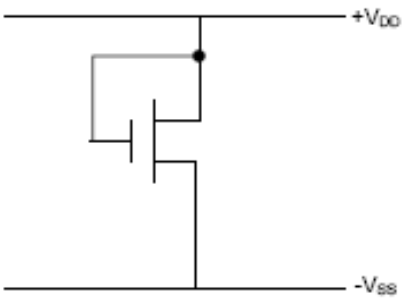

Fig.3: Test circuit for saturation region model verification: a diode connected transistor

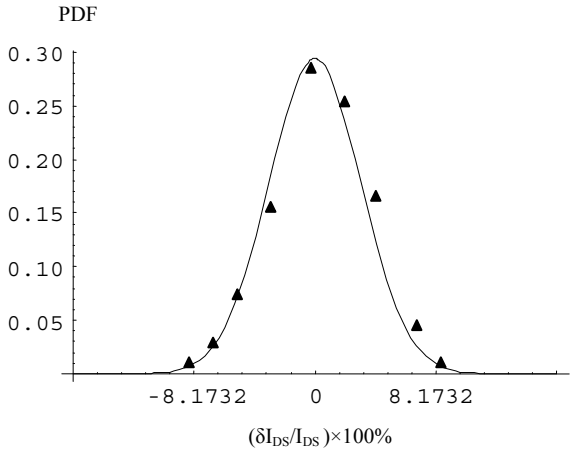

Fig.4: Saturation region PDF comparison: estimated PDF from the model (line), actual PDF from the test circuit (▲)

4. Discussion

Before proceed to the conclusion, some discussions are worthy to be mentioned. Since the voltage conditions for triode and saturation region are $V_{ds} < V_{gs} - V_t$ and $V_{ds} \geq V_{gs} - V_t$ respectively, (5) and (11) can be combined into a single probability density function as follows

$$f_{\Delta I_{ds}}(\delta I_{ds}) = \begin{cases} \dfrac{(V_{ds} + \mu^{-1} L v_{sat}) WL}{4\sqrt{2\pi} A_{Vt}^2 W C_{ox} V_{ds} v_{sat}} \\ \times \exp\left[-\dfrac{(V_{ds} + \mu^{-1} L v_{sat}) WL \delta I_{ds}^2}{16 A_{Vt}^2 W C_{ox} V_{ds} v_{sat}} \right]; V_{ds} \geq V_{gs} - V_t \\ \dfrac{WL}{\sqrt{2\pi} (W C_{ox} v_{sat} A_{Vt})^2} \\ \times \exp\left[-\dfrac{WL \delta I_{ds}^2}{2 (W C_{ox} v_{sat} A_{Vt})^2} \right]; V_{ds} \geq V_{gs} - V_t \end{cases} \tag{19}$$

Furthermore, a few examples of further studies are also worthy to be discussed. These examples are trying to apply the other models of variation in ΔV_t such as those proposed in [2], [3] and [4] in order to obtain the alternative results, inclusion of the other process induced random variations apart from ΔV_t such as the random variation in μ ($\Delta\mu$) etc., in order to obtain more precise models, performing the similar study to the weak inversion operated transistor as this study has been performed by assuming the strong inversion operation and derivation of the similar models for the random variations in the other related parameters for example, g_m, g_{mb} and r_{ds} etc., similarly to [6].

5. Conclusion

The probabilistic models of random variation in I_{ds} which is a key parameter of any MOS transistor, for both triode and saturation regions have been proposed in this research by using the up to dated nanoscale regime MOS equations as bases. The proposed models have been verified at 65 nm technology by using the Monte Carlo simulation and the KS-test. The chosen test circuits are a single transistor active resistor and a diode connected transistor for the triode and saturation region model respectively. These models are very accurate since they can fit the random variation in I_{ds} obtained from the test circuits with 99% confidence. Hence, the proposed models are obviously efficient for the statistical/variability aware design of various nanoscale CMOS analog/mixed signal circuits and systems.

6. Acknowledgement

The author would like to acknowledge Mahodol University, Thailand for online database service.

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