

The Ethernet Network Manipulative System based on RTL8019AS

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Abstract—The Ethernet network is widely used in industry. A practical design of using the abundant resource of Ethernet is introduced, which applies RTL8019AS to set up a microoperation system. The cost of this system is cheap and simple to realize.

Keywords- Ethernet RTL8019AS Industry

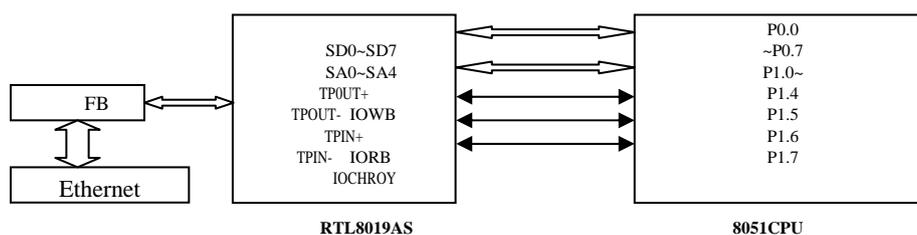
1. Introduction

With the rapid development of network technology, it has been widely used in many industrial field. The original Ethernet was developed as an experimental coaxial cable network in the 1970s by Xerox Corporation to operate with a data rate of 3 Mbps using a carrier sense multiple access collision detect (CSMA/CD) protocol for LANs with sporadic but occasionally heavy traffic requirements. Success with that project attracted early attention and led to the 1980 joint development of the 10-Mbps Ethernet Version 1.0 specification by the three-company consortium: Digital Equipment Corporation, Intel Corporation, and Xerox Corporation. The original IEEE 802.3 standard was based on, and was very similar to, the Ethernet Version 1.0 specification. The draft standard was approved by the 802.3 working group in 1983 and was subsequently published as an official standard in 1985 (ANSI/IEEE Std. 802.3-1985). Since then, a number of supplements to the standard have been defined to take advantage of improvements in the technologies and to support additional network media and higher data rate capabilities, plus several new optional network access control features. System fabric is showed as Fig. 1.

2. NETWORK realization

The simplest Ethernet structure is the point-to-point interconnection. Only two network units are involved, and the connection may be DTE-to-DTE, DTE-to-DCE, or DCE-to-DCE. The cable in point-to-point interconnections is known as a network link. The maximum allowable length of the link depends on the type of cable and the transmission method that is used. ^[1]

As with all IEEE 802 protocols, the ISO data link layer is divided into two IEEE 802 sublayers, the Media Access



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Fig.1. The system structure

Control (MAC) sublayer and the MAC-client sublayer. The IEEE 802.3 physical layer corresponds to the ISO physical layer. The MAC-client sublayer may be one of the following: Logical Link Control (LLC), if the unit is a DTE. This sublayer provides the interface between the (1) Ethernet MAC and the upper layers in the protocol stack of the end station. The LLC sublayer is defined by IEEE 802.2 standards. (2) Bridge entity, if the unit is a DCE. Bridge entities provide LAN-to-LAN interfaces between LANs that use the same protocol (for example, Ethernet to Ethernet) and also between different protocols (for example, Ethernet to Token Ring). Bridge entities are defined by IEEE 802.1 standards. (3) Because specifications for LLC and bridge entities are common for all IEEE 802 LAN protocols, network compatibility becomes the primary responsibility of the particular network protocol.^{[2][3]}

Whenever an end station MAC receives a transmit-frame request with the accompanying address and data information from the LLC sublayer, the MAC begins the transmission sequence by transferring the LLC information into the MAC frame buffer. (1) The preamble and start-of-frame delimiter are inserted in the PRE and SOF fields. (2) The destination and source addresses are inserted into the address fields. (3) The LLC data bytes are counted, and the number of bytes is inserted into the Length/Type field. (4) The LLC data bytes are inserted into the Data field. If the number of LLC data bytes is less than 46, a pad is added to bring the Data field length up to 46. (5) An FCS value is generated over the DA, SA, Length/Type, and Data fields and is appended to the end of the Data field. After the frame is assembled, actual frame transmission will depend on whether the MAC is operating in half-duplex or full-duplex mode. The IEEE 802.3 standard currently requires that all Ethernet MACs support half-duplex operation, in which the MAC can be either transmitting or receiving a frame, but it cannot be doing both simultaneously. Full-duplex operation is an optional MAC capability that allows the MAC to transmit and receive frames simultaneously.

The RTL8019AS is a highly integrated Ethernet Controller which offers a simple solution to implement a Plug and Play NE2000 compatible adapter with full-duplex and power down features. With the three level power down control features, the RTL8019 is made to be an ideal choice of the network device for a GREEN PC system. The full-duplex function enables simultaneously transmission and reception on the twisted-pair link to a full-duplex Ethernet switching hub. This feature not only increases the channel bandwidth from 10 to 20 Mbps but also avoids the performance degrading problem due to the channel contention characteristics of the Ethernet CSMA/CD protocol. The Microsoft's Plug and Play function can relieve the users from pains of taking care the adapter's resource configurations such as IRQ, I/O, and memory address, etc. However, for special applications not to be used as a Plug and Play compatible device, the RTL8019 also supports the jumper and proprietary jumperless options. To offer a fully plug and play solution, the RTL8019AS provides the auto-detect capability between the integrated 10BaseT transceiver, BNC and AUI interface. Besides, the 10BaseT transceiver can automatically correct the polarity error on its receiving pair. Furthermore, 8 IRQ lines and 16 I/O base address options are provided for grand resource configuration flexibility. The RTL8019AS supports 16k, 32k & 64k byte BROM and flash memory interface. It also offers the page mode function which can support up to 4M-byte BROM within only 16k-byte system memory space. Besides, the BROM disable command is provided to release the BROM memory space for other system usage after the BROM program is loaded. The RTL8019AS is built in with 16K-byte SRAM in a single chip. It is designed not only to provide more friendly functions but also to save the effort of SRAM sourcing and inventory.^[4]

The RTL8019AS's resource configuration informations such as I/O base address, BROM memory base address, and interrupt request line, etc., are stored in the CONFIG3-0 registers in Group1 as well as the PnP logical device configuration registers. Their power-up default values may come from the states of jumper pins in jumper mode or the contents of 9346 in PnP and RT jumperless mode. Their values can be modified by software via the logical device configuration registers in all 3 modes. The update values will be recorded to the CONFIG3-0 registers, too. This new configuration is only valid temporarily and will be lost after an auto-load command, an active RSTDRV, or PC power off. Permanent changes of configuration must be done by changing the jumper states or the contents of 9346. Note that the BROM size can not be modified temporarily.

The Plug and Play logic can work in all the three configuration modes except that an RT defined initiation key, named RT initiation key, should be used instead of the PnP initiation key. In other words, the RT

initiation key is supported in all configuration modes while the PnP initiation key is only supported in the PnP mode. By using the RT initiation key, the software can put RTL8019AS to the PnP Config state and access the logical device configuration registers even in the jumper and RT jumperless modes. The Plug and Play logic is quiescent on power up and must be enabled by software. This is done by a predefined series of writes (32 I/O writes) to the ADDRESS port, which is called the initiation key. The write sequence is decoded by RTL8019AS. If the proper series of I/O writes is detected, then the Plug and Play auto-configuration ports are enabled. The write sequence will be reset and must be issued from the beginning if any data mismatch occurs. The exact sequence for the initiation key is listed below in hexadecimal notation.

The hardware protocol can be invoked by the Plug and Play software at any time. The initiation key described earlier, puts all cards into configuration mode. The hardware on each card expects 72 pairs of I/O read accesses to the READ_DATA port. The card's response to these reads depends on the value of each bit of the serial identifier which is being examined one bit at a time. If the current bit of the serial identifier is a "1", then the card will drive the data bus to 55H to complete the first I/O read cycle. If the bit is "0", then the card puts its data bus driver into high impedance. All cards in high impedance will check the data bus during the I/O read cycle to sense if another card is driving SD[1:0] to "01". During the second I/O read, the card(s) that drove the 55H, will now drive a AAH. All high impedance card will check the data bus to sense if another card is driving SD[1:0] to "10." If a high impedance card sensed another card driving the data bus with the appropriate data during both cycles, then that card ceases to participate in the current iteration of card isolation. Such cards, which lose out, will participate in future iterations of the isolation protocol. If a card was driving the bus or if the card was in high impedance and did not sense another card driving the bus, then it should prepare for the next pair of I/O reads. The card shifts the serial identifier by one bit and uses the shifted bit to decide its response. At the end of this process, one card remains. This card is assigned a handle referred to as the Card Select Number (CSN) that will be used later to select the card. Cards which have been assigned a CSN will not participate in subsequent iterations of the isolation protocol. Cards must be assigned a CSN before they will respond to the other PnP commands.^[5]

The Plug and Play software sends the initiation key to all Plug and Play cards to place them into configuration mode. The software is then ready to perform the isolation protocol. The Plug and Play software generates 72 pairs of I/O read cycles from the READ_DATA port. The software checks the data returned from each pair of I/O reads for the 55H or AAH driven by the hardware. If both 55H or AAH are read back, then the software assumes that the hardware had a "1" bit in that position. All other results are assumed to be a "0". During the first 64 bits, software generates a checksum using the received data. The checksum is compared with the checksum read back in the last 8 bits of the sequence.

3. Conclusions

The system based on Ethernet control system has a widely application prospect and it is developing to integration, intelligibility and modularization.

4. References

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