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A Novel PSR Enhancement Technique for Full on-Chip Low-Dropout Regulator

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Abstract. A novel feedback-factor-control (FFC) technique is presented to improve mid-frequency power supply rejection (PSR) of full on-chip low dropout regulator (LDO). With this method, the zeros of PSR are rearranged in a nested Miller compensation (NMC) based full on-chip LDO. The mid-frequency PSR is enhanced when the dominant zero of PSR is moved to higher frequency by FFC circuit. The full on-chip LDO implemented with Chartered 0.35μm CMOS process, features almost -90dB PSR at 10 kHz and about -45dB at 1MHz. When the load current changed from 0.5mA to 50mA, the maximum output-voltage variation is less than 70mV.

Keywords: low dropout regulator; full on-chip; power-supply rejection.

1. Introduction

With the rapid development of RF system-on-chip (SoC), power supply noise attracts more and more concentration. A typical LDO usually needs a large off-chip output capacitor, which makes it not suitable for SoC designs [1]. Recently, full on-chip LDO has been widely developed; however, it suffers from poor mid-frequency PSR. Numerous techniques have been used to overcome this issue [2]-[6]. One is using cascading two regulators [4], but this leads to a high drop-out voltage. Another method is using a feedforward ripple cancellation (FFRC) technique [5]. The drawback is that a 4μF off-chip capacitor is still required, too large to apply in SoC applications. Cascading an NMOS to the PMOS pass device of LDO is another solution [6], in which the NMOS is boosted using a charge pump. However, the using of the charge pump increases quiescent current, and reduces the efficiency.

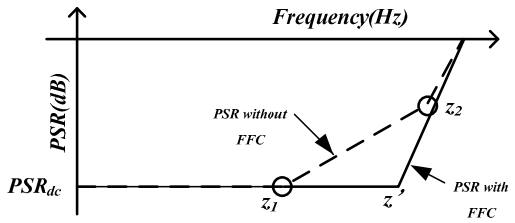

Figure 1. The PSR characteristics diagram with FFC and without FFC

To improve mid-frequency PSR of full on-chip LDOs, a novel feedback-factor-control (FFC) technique is presented in this paper. The PSR characteristics diagram with FFC and without FFC is shown in Fig.1. By controlling the feedback factor, the two zeros z_1 and z_2 are forced to combine a zero-doublet z', which can be moved to higher frequency, resulting in improving the mid-frequency PSR.

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2. System Design and Analysis

2.1 PSR of full on-chip LDO with traditional NMC

Fig.2 shows the basic structure of LDO with the traditional NMC [7][8]. The PSR transfer function is

$$PSR = \frac{v_{out}}{v_{dd}} \approx \frac{s^2 g_{mp} C_{gd} C_m + s\frac{g_{mp}}{r_{o1}} C_{gd} + \frac{1}{r_{o1} r_{o2} r_{ds}}}{s^2 g_{mp} C_{gd} C_m + s g_{m2} g_{mp} C_m + g_{m1} g_{m2} g_{mp} \beta} \tag{1}$$

where $\beta = v_{fb}/v_{out}$, is the feedback factor of PSR path. g_{mp}, r_{ds} and C_{gd} are the transconductance, channel resistance and gate-drain capacitor of the power transistor. C_m is a Miller compensation capacitor fed back to the output of the first stage. g_{m1}, g_{m2}, r_{01} and r_{02} are the transconductance of the first stage amplifier, the transconductance of the second stage amplifier, the output resistance of the first stage, and the output resistance of the • second stage, respectively.

Here, β is denoted by β_0

$$\beta_0 = \frac{R_{f2}}{R_{f1} + R_{f2}} \tag{2}$$

We have

$$PSR_{dc} = \frac{1}{g_{m1} g_{m2} g_{mp} r_{o1} r_{o2} r_{ds} \beta} = \frac{1}{A_{lp\_dc}} \tag{3}$$

$$z_1 = -\frac{1}{g_{mp} r_{o2} r_{ds} C_{gd}}, \quad z_2 = -\frac{1}{r_{o1} C_m}$$

$$p_1 = -\frac{\beta_0 g_{m1}}{C_m}, \quad p_2 = -\frac{g_{m2}}{C_{gd}} \tag{4}$$

where $A_{lp\text{-}dc}$ is the DC loop gain. Obviously, at low frequencies, PSR is determined by the DC loop gain.

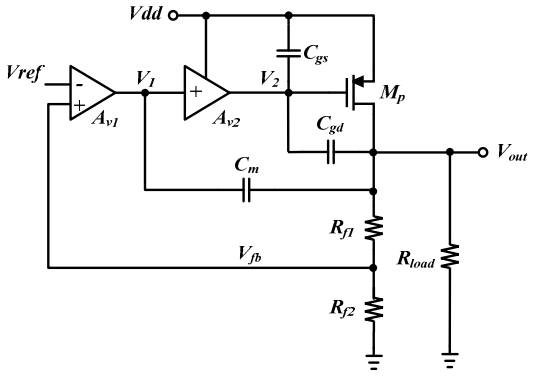

Figure 2. Basic LDO regulator with traditional NMC structure circuit

Since poles are much greater than zeros, only zeros are considered in following discussions. Clearly, $z_1 << z_2$, leads to low mid-frequency PSR, shown in Fig.1 with dash line. However, if we push the dominant zero z_1 to higher frequency, the mid-frequency PSR can be improved.

2.2 The Proposed LDO With FFC

To boost the mid-frequency PSR of the circuit, the proposed FFC circuit is introduced, shown in Fig. 3. The small signal for PSR equivalent circuit is indicated in Fig. 4.

With FFC circuit,

$$\beta = \frac{v_{fb}}{v_{out}} = \beta_0 + \frac{(R_{f1} // R_{f2})[g_{mf3}(r_{of1} - r_{of2}) + sC_f r_{of1}]}{r_{of1} r_{of2}(g_{mf3} + sC_f)} \cdot \frac{v_{dd}}{v_{out}} \tag{5}$$

where g_{mf3} is the transconductance of M_{f3}.

For simplicity, equation (1) and (5) are written as

$$\frac{v_{out}}{v_{dd}} = \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0 \cdot \beta} \tag{6}$$

$$\beta = \beta_0 + \frac{c_1 \cdot s + c_0}{d_1 \cdot s + d_0} \cdot \frac{v_{dd}}{v_{out}} \tag{7}$$

where,

$$a_2 = g_{mp} C_{gd} C_m, a_1 = \frac{g_{mp}}{r_{o1}} C_{gd}, a_0 = \frac{1}{r_{o1} r_{o2} r_{ds}},$$

$$b_2 = g_{mp} C_{gd} C_m, b_1 = g_{m2} g_{mp} C_m, b_0 = g_{m1} g_{m2} g_{mp},$$

$$c_1 = \frac{(R_{f1} // R_{f2}) C_f}{r_{of2}} \quad c_0 = \frac{g_{mf3}(R_{f1} // R_{f2})(r_{of1} - r_{of2})}{r_{of1} r_{of2}},$$

$$d_1 = C_f, d_0 = g_{mf3}$$

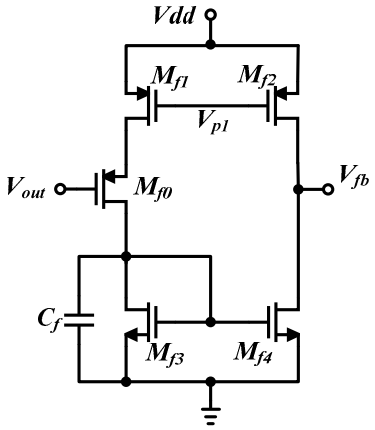

Figure 3. FFC circuit structure

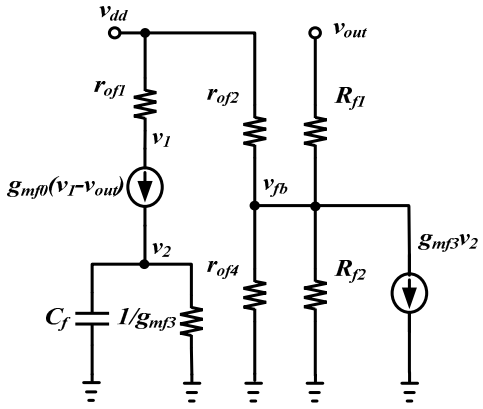

Figure 4. Small signal mode for PSR of FFC circuit

Therefore, the final system PSR is

$$PSR = \frac{v_{out}}{v_{dd}} \approx$$

$$\frac{s^2 \cdot (a_2 d_0 + a_1 d_1) + s \cdot (a_1 d_0 + a_0 d_1 - b_0 c_1) + d_0 (a_0 - \alpha)}{(s^2 \cdot b_2 + s \cdot b_1 + b_0 \cdot \beta_0)(d_1 \cdot s + d_0)} \tag{8}$$

where $\alpha = b_0 c_0 / d_0 > 0$ is introduced by FFC. Therefore, the feedback factor β can be controlled by varying α to obtain a higher mid-frequency PSR.

1) ***PSR at low frequencies***

From equation (8), system PSR at low frequencies is expressed by

$$PSR_{dc} = \left| \frac{a_0 - \alpha}{b_0 \beta_0} \right| \tag{9}$$

a) Heavy load

When the load current is large, $a_0 - \alpha$ is positive; therefore, $PSR_{dc} = (a_0 - \alpha)/(b_0 \beta_0)$. Larger α will lead to higher PSR at low frequencies.

b) Light load

This situation is exactly opposite with heavy load. In order to obtain higher low frequency PSR at light load, α should be small.

2) ***Zeros of PSR***

In order to analyze the zeros of PSR, we have to simplify the expression. The discriminant of the numerator in equation (8) is

$$\Delta = (a_1 d_0 + a_0 d_1 - b_0 c_1)^2 - 4 d_0 (a_2 d_0 + a_1 d_1)(a_0 - \alpha) \tag{10}$$

a) Heavy load

Large load current results in positive a_0-α. Thus, Δ is negative, introducing a pair of complex conjugate zeros in PSR

$$z_{complex} = \sqrt{\frac{a_0 - \alpha}{(a_2 + a_1 \frac{d_1}{d_0})}} \tag{11}$$

It can be observed that complex zero can be increased by decreasing α.

b) Light load

With this condition, a_0-α is negative and the Δ is positive, leading to two real zeros

$$z_{1,2} = -\frac{(a_1 d_0 + a_0 d_1 - b_0 c_1) \mp \sqrt{\Delta}}{2(a_2 d_0 + a_1 d_1)} \tag{12}$$

z_1 can be increased by reducing α, z_2 can be increased by increasing α.

From the analysis above, it's important to note that both the value of low frequency PSR and the frequency of zeros in PSR curve all are dependent on α. There is a trade-off between them. In order to obtain a better PSR characteristic in full load range, we have to sacrifice the low-frequency PSR.

In addition, the system frequency response feedback factor is

$$\frac{v_{fb}}{v_{out}} \approx \frac{R_{f2} // r_{of2} // r_{of4}}{R_{f1} + R_{f2} // r_{of2} // r_{of4}} \approx \frac{R_{f2}}{R_{f1} + R_{f2}} \tag{13}$$

This is to say, if r_{of2}, $r_{of4} >> R_{f1}$, R_{f2} is satisfied, the influence of FFC circuit on the system stability can be ignored.

3. Circuit Implementation and Simulation Results

The proposed LDO is composed of a two-stage amplifier, a power transistor, feedback resistors and FFC circuit, as shown in Fig.5. In order to achieve a good transient response of LDO, the second stage amplifier

utilizes gm-boosting circuit [9]. To meet the condition r_{of2}, r_{of4} >>R_{f1}, R_{f2}, a cascade structure is used. Meanwhile, a source follower stage is used to guarantee normal operation of M_{f0}.

Fig.6 shows that the PSR performance of the LDO with (solid line) and without FFC (dashed line) with 50mA load current. The low frequency PSR increases 6dB. It is clear to see that there is a pair of the complex zero, located between the low frequency zero and the high frequency zero of the LDO without FFC, which introduces a 36dB increasing of PSR at the middle frequency.

Just like predicted in equation (12), at the light load, for example, 0.5mA, there are two real zeros on the PSR curve. Compared with the zeros without FFC, the two zeros are tending to combine together at the light load condition, as seen from the Fig.7, resulting in the mid-frequency PSR boosting about 28dB. However, the penalty is that the low-frequency PSR with FFC (solid line) is 6dB lower than that of without FFC (dashed line).

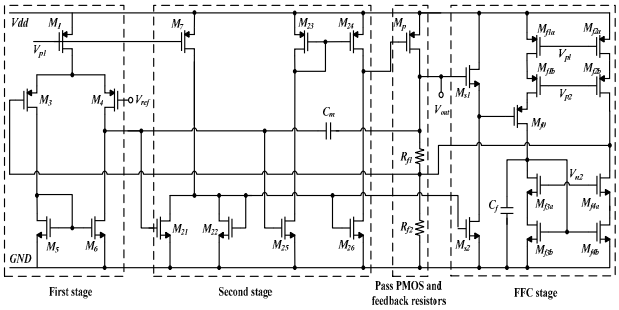

Figure 5. Proposed LDO regulator

Even so, since the DC loop gain of the system is high enough when the load current is low, the low-frequency PSR can be maintained a high value. It can be seen from the Fig.7 that the low frequency PSR is still higher than 95dB.

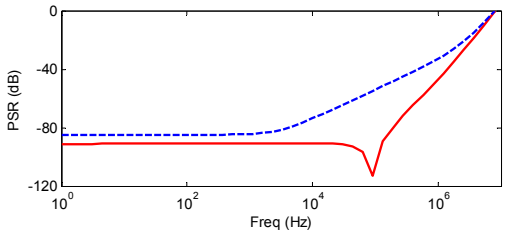

Figure 6. Comparison of PSR between LDOs with and without FFC with 50mA load current.

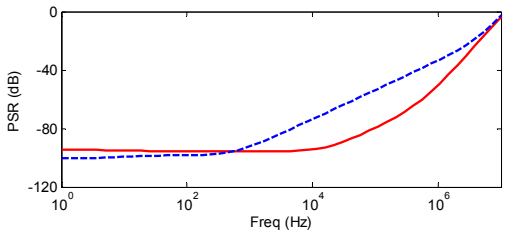

Figure 7. Comparison of PSR between LDOs with and without FFC with 0.5mA load current.

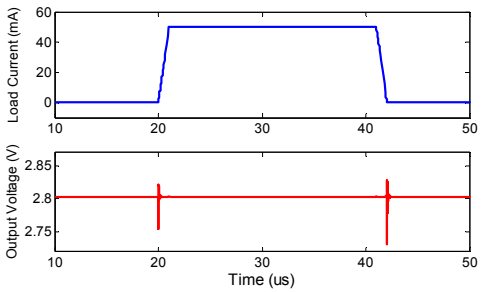

Figure 8. Load transient response of the proposed LDO.

Fig.8 illustrates the transient response. When the load current is changed from 0.5mA to 50mA and back to 0.5mA in 1μs, the overshoot and undershoot of this LDO is 35mV and 70mV, respectively.

4. Conclusions

A full on-chip CMOS LDO with high mid-frequency PSR is presented in this paper, based on the FFC circuit. The proposed LDO not only improves the mid-frequency PSR, but also occupies smaller chip area. With total internal compensation capacitors as small as 0.5pF, -90dB PSR at 10 kHz and about -45dB at 1MHz are achieved for this full on-chip LDO. Therefore, the proposed structure offers a good choice for the design of full on-chip power management.

5. Acknowledgment

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