2010 3rd International Conference on Computer and Electrical Engineering (ICCEE 2010)
IPCSIT vol. 53 (2012) © (2012) IACSIT Press, Singapore
DOI: 10.7763/IPCSIT.2012.V53.No.1.51

The Routing Strategy of Network-on-Chip with Dual Subnets Infrastructure

Hui Shen+ and Xiang Ling

National Key Laboratory of Science and Technology on Communication
University of Electronic Science and Technology of China
Chengdu, 611731, P. R. China

Abstract. For avoiding transmission congestions in Network-on-chip (NoC) under XY routing mechanism, this paper proposes a dual subnets mesh network structure to dispatch packets into these two subnets. In each subnet, XY routing and YX routing are adopted respectively to keep deadlock free. With the same total size of router buffers, this NoC infrastructure and routing strategy greatly improve the throughput and transmission delay at the cost of moderate increasing bus width.

Keywords: Network on chip (NoC); dual subnets; XY-YX hybrid route; deadlock;

1. Introduction

With the deep sub-micron process level enhancement, the VLSI feature size is reduced, making the interconnection between on-chip resources the most critical factor in the system-on-chip design for delay and power constraints. Therefore, network–on-chip (NoC) becomes the promising solution in enhancing the communication efficiency of system-on-chip. Compared with conventional on-chip bus communication, on-chip network has several advantages: 1) as the reusable design, on-chip network has good scalability; 2) physical link length and delay can be better handled.

Switching strategy of NoC determines how the data runs through its chosen path in NoC. There are two basic switching strategies: circuit switching and packet switching. For packet switching networks, there are three methods: store-and-forward mode, virtual cut-through mode and wormhole mode.

Generally, the data delay is composed of two parts. One part is the packet transmitting delay on links, and the other part is processing delay in routers. In practice, the length of data packet is far larger than the delay due to route processing of every node, so delay is mainly decided by the former part. Wormhole switching requires little space for router buffer cache, so it greatly reduces the transmitting time of data packet in each hop. The key idea in wormhole switching is to divide the data packet into multiple micro-chips (flit), the first flit carries the routing information, and the remained filts move forward in network like water flow according to the paths that the first flit chooses. When obstruction occurs, each flit is temporarily stored in the node where it is travelling. In this way, each router only requires very little cache space for buffering only a few flits instead of buffering the whole data packet. Thus a compact router with high speed can be constructed.

However, there is a big drawback in wormhole switching since the routing algorithm based on wormhole switching is sensitive to network jamming. Wormhole switching doesn't release node resources during transmission process. Once a channel starts to transmit the first flit of a data packet, it is occupied by the packet until all the remaining flits are transmitted. When one packet is jammed, it affects all nodes where this packet's

+ Corresponding author.
E-mail address: huihui_uestc@126.com.

flits lingered by occupying the buffer duratively. Thus causes more serious jamming since other packet transmission will be paused if they can not get the resources from these nodes.

2. Transmission of Dual Subnets

2.1 Deadlock problem

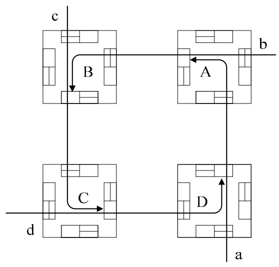


Fig. 1. Deadlock within four nodes

Due to divide into multiple flits, a data packet will occupy several intermediate nodes. And a loop may be formed among several data packets or several flits of one data packet. Therefore, none of the data packets can move forward to the next router. Fig. 1 shows the scenario with four data packets (indexed by a, b, c and d) and four routers (indexed by A, B, C and D). Packet a occupies the physical link from D to A and is applying for the west output port of router A. However, the west output port of router A is occupied by packet b, so packet a is waiting for packet b to release the resource. Packet b occupies the physical link from router A to B, and is applying for south output port of router B which is currently used by packet c. so packet b will wait for packet c to release resource. In the same way, packet c is waiting for packet d to release the east output port of router C and packet d is waiting for packet a to release north output port of router D. Four packets all need resources and can not move forward. Therefore, deadlock occurs. The reason for deadlock is that a resource logically relates to channel, and data packets are constrained by dependency of channel resources when passing through network. So to solve deadlock problem, the dependency of closed loop of channel resources needs to be broken.

Generally there are three ways to avoid deadlock:

a) Limiting some routing direction and breaking potential resource dependency loop when designing routing algorithms.

b) Virtual channels (VC)

c) Deadlock detection and mandatory destruction of resource dependency ring.

This paper resolves the deadlock problem by combining the former two methods.

2.2 On-chip network system

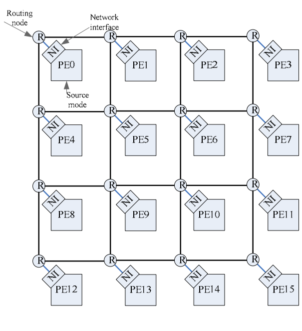


Fig. 2. Mesh topology of NoC

The routing strategy discussed here is based on mesh topology which is shown in Fig. 2. The mesh NoC is composed of routers (R), link (L), network interface (NI), and local system (LS). Router is the core component of network. Local system consists of processing element (PE) and private memory. PE accesses private memory through local bus, and connects network by NI. Data transmission path among PEs is

PE->NI->routers->routers->NI->PE. NoC usually adopts *global asynchronous local synchronous* (GALS) mechanism.

In the wormhole routing, the arbiter selects the forward direction once the head flit enters a router, and establishes transmission path and assigns resources. The following flits of the data packet moves forward along the path determined by head flit. When all the flits are transmitted, resources are released.

Specific routing process includes three basic operations: routing computing (RC), virtual channel allocation (VCA) and crossbar traversal (CT).

Dimension-ordered routing is a simple way to avoid deadlock. Data packet is routed along one dimension firstly. For example, column-first means routing along column till the target row approached, and then along the row direction to the target column, thus arriving at the destination node. This way can avoid deadlock. But it is a kind of deterministic routing. The packets with the same column or same row are always routed on the same route, and can not avoid congestion. When congestion occurs, packets have no ability to alter the transmission direction and have to wait until the channels are available. However, network is hard to be recovered from congestion, which will increase the transmission delay. XY routing algorithm is one of dimension-ordered routing, by which flits move forward along X direction and then Y direction. XY routing suffers from traffic congestion problem too.

2.3XY-YX routing based on dual subnets

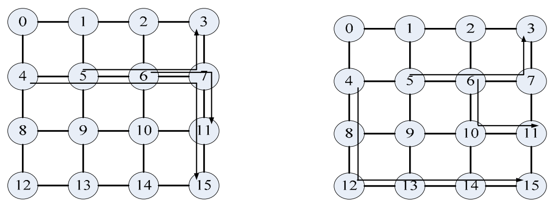
Source routing is usually considered in parallel computer network. Source node sets up data packet header, which includes node number of each router along the transmission path. Each router simply picks up node number from message header, and forwards the message through channels specified by crossbar. The routed path of data packets is determined at the very beginning. This routing method is simple to be implemented even in complex topologies since routing computation unit is not needed.

The basic idea of XY routing algorithm is to move forward along X direction and then Y direction. Although it is deadlock-free, it can cause obstruction. Because data reaches any target node after they starts in X direction, either through east channel or west channel. If multiple data packets are transmitted along the same X direction, then the east channel or west channel is easily blocked, thus greatly increasing the packet delay and reducing the throughput. One of the blocking situations is formulatd clearly in Fig. 3(a). The node 4 sends data to node15, and at the same time node 5 send data to node 3, and node 6 send data packets to node 11. We can see that the X direction link between node 4and 7 can easily be congested.

In order to solve the problem in XY routing, this paper proposes XY-YX hybrid routing in dual subnets, which chooses XY or YX routing for data packets according to the relative position of source and destination node, and two subnets transmitting the packets by XY an YX routing respectively. In this way, the extreme congestion problem in Fig. 3(a) can be resolved. We use direction algorithm to escape the congestion situation. Then the traffic will be dispersed to different dimensions, as shown in Fig. 3(b).

But when the network uses both XY routing and YX routing, it will bring in deadlock problem. So a network structure with dual subnets is proposed in this paper. The mesh network with dual subnets is shown is Fig. 4 with independent data transmissions between link 1 and link 2.

PE sends data to NI, and NI determines whether XY or YX routing is taken according to the relative position of source node and destination node. And all the data packets will be stored into XY-NI buffer and YX-NI buffer according to their selected routing way. The VCs in routers are divided into XY-VC and YX-VC and are assigned for XY routing and YX routing, respectively. The number of links between routers in this strategy is twice of that in conventional NoCs.



(a) The congestion of XY routing (b)Solve the congestion by XY-YX routing

Fig. 3. XY-YX hybrid routing dispatch the packets in different directions to relieve the congestion

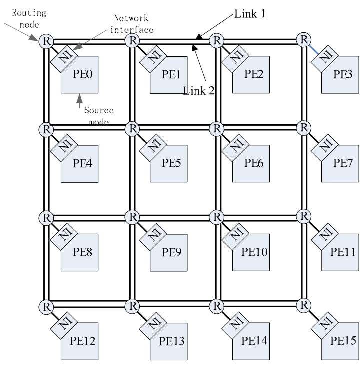


Fig. 4. The mesh network with dual subnets

The dual subnets requires not only the increasing number of physical links between routers, but also the modifications of NIs and routers, thus making the data packets move forward independently in XY subnet and YX subnet.

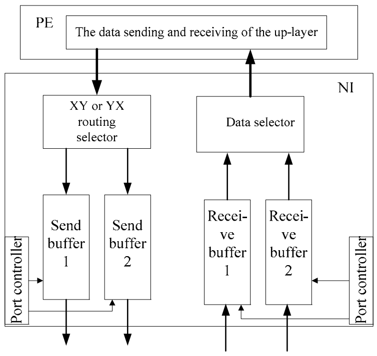


Fig. 5. NI structure for dual subnets

As shown in Fig. 5, NI for dual subnets at first examines the data from PE and extracts its target address, and decides whether XY routing or YX routing is taken according to the relative position of source node and destination node. With this routing strategy, NI adds the pre-assigned intermediate node number into the packet header. And then packet header and end flag is added. Finally, the processed data packet is stored into sending buffer 1 or 2 of NI. NI receiver separately stores the data from XY routing and YX routing, and then data selector module sends the data to PE module for further processing.

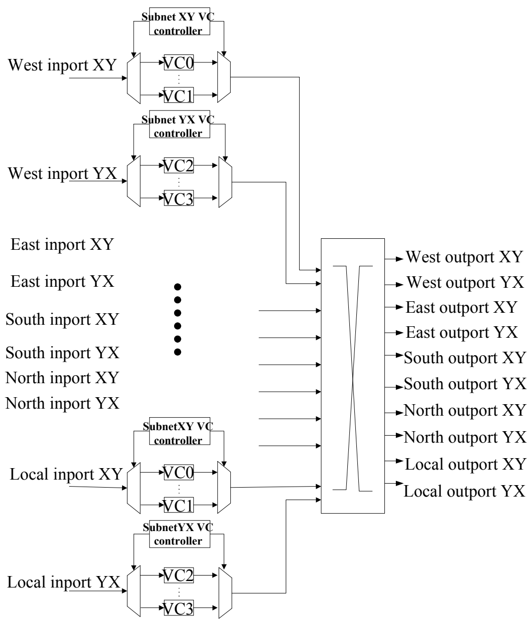


Fig. 6. Router structure of dual subnets

Some corresponding modifications of router in dual subnets have to be made so that data packets can be sent independently and quickly, as shown in Fig. 6. When new data packet enters the router, the router will examine whether the data packet is in XY subnet or YX subnet. And then in-charge port controller will forward the data. By dividing the input virtual channels into two parts, VC0 and VC1 only accept the data packets in XY subnet, and VC2 and VC3 only accept the data packets in YX subset. The four VCs in router and two links connected split the whole mesh network into two subnets.

2.4 The criteria for subnets choice

In XY-YX routing strategy in dual subnets, physical ring does exist from the whole network's perspective. Deadlock will be avoided, because the two subnets don't have a ring in their respective networks. To be specific, data packets in XY subnet follow the XY routes and data packets in another follow the YX routes.

The dual subnets transmit the packet by XY routing or YX routing. Which subnet will be chosen is depended on the source and destination address of data packets. One important objective for subnet choice is to distribute the data packets onto these two subnets uniformly, so that the packets with different source and destination pair will not concentrate on the same column or row. This paper proposes direction algorithms for subnet choice based on above criteria.

Direction algorithm:

Step 1: if x coordinate of source and destination nodes are the same, then choose XY routing.

Step 2: if y coordinate of source and destination are the same, then select YX routing.

Step 3: if $x_d < x_s$ and $y_d > y_s$ (northwestern direction), or if $x_d > x_s$ and $y_d < y_s$ (southeastern direction), then choose XY subnet.

Step 4: if $x_d < x_s$ and $y_d < y_s$ (southwestern direction), or if $x_d > x_s$ and $y_d > y_s$ (northeastern direction), then select YX subnet.

3. Simulation Result

Our design is tested in MSNS simulator [8] which is based on systemC for basic description and integration. The systemC has high simulation speed and can do simulation for both hardware and software.

In simulation, wormhole switching is adopted. The flit size is 1 Bytes. The traffic arrival rate follows Poisson distribution. The transmission delay and throughput performance are compared for conventional algorithm and the proposed mechanism in mesh network.

Table 1. Buffer Resources Consumptions

	NI		Router	
	The number of buffers per port	Buffer size(Byte)	The number of buffers per port	Buffer size(Byte)
Conventional mesh network	1	65534	2	4
Dual subnets mesh network	2	32767	4	2

As shown in Table 1, the total buffer capacity needed of dual subnets is the same as that of conventional mesh network. Thus, more link source is the only penalty for our design than the conventional NoC network.

In Poisson distribution, the time interval between two adjacent injection events follows exponential distribution with parameter λ. The time interval can be obtained by the probability density function of exponential distribution

$$F(x) = \begin{cases} \int_{-\infty}^{x} f(y)\,dy = 1 - e^{-\lambda x}, x \ge 0 \\ 0, x < 0 \end{cases}. \quad (1)$$

During simulation, PE generates the data packets according to Poisson distribution. Then the packets are injected into the buffer of NI, and NI injects the flits into the dual subnets.

In our simulation, our proposed algorithm outperforms the conventional one under the three scenarios: the extreme congested traffic mode, the uniform traffic mode and hot-spot traffic mode.

Extreme congested traffic means the traffic in some X direction or Y direction link is very heavy, just as shown in Fig. 7(a). The sending nodes and receiving nodes are pre-selected.

Uniform traffic means to select some sending nodes randomly. In this case, sending nodes and receiving nodes have a one-to-one correspondence. One sending node only sends data to a specified receiving node, while the receiving node only receives data from the sending node. These sending-receiving node pairs are randomly selected.

Hot-spot traffic means one receiving node can send data to multiple receiving nodes. And the node from the multiple receiving nodes for actually receiving data is randomly selected every time a data packet arrives.

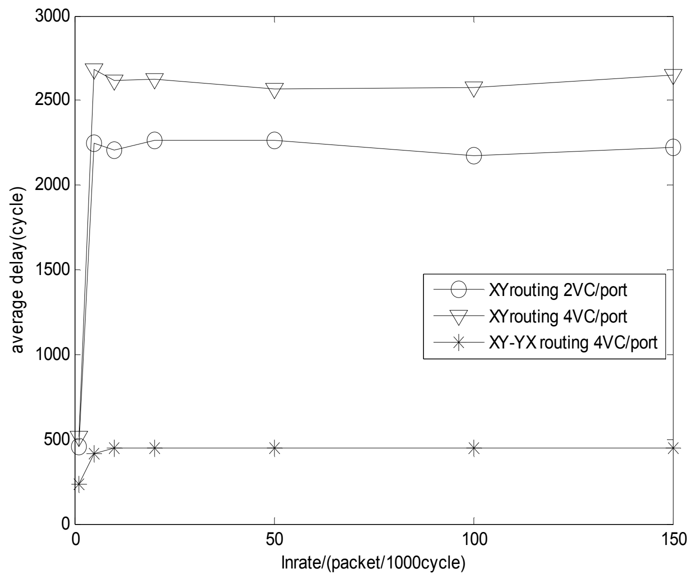


Fig. 7(a). The delays in extreme congested traffic scenario for traditional NoC and XY-YX dual subnets NoC

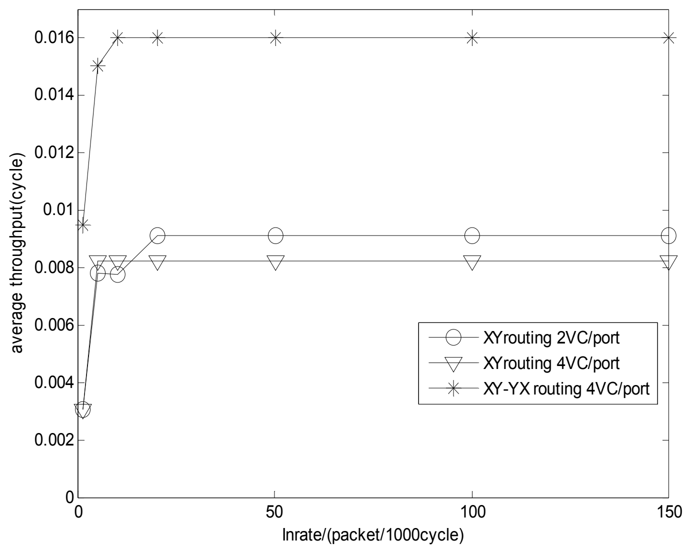


Fig. 7(b). The throughputs in extreme congested traffic scenario for traditional NoC and XY-YX dual subnets NoC

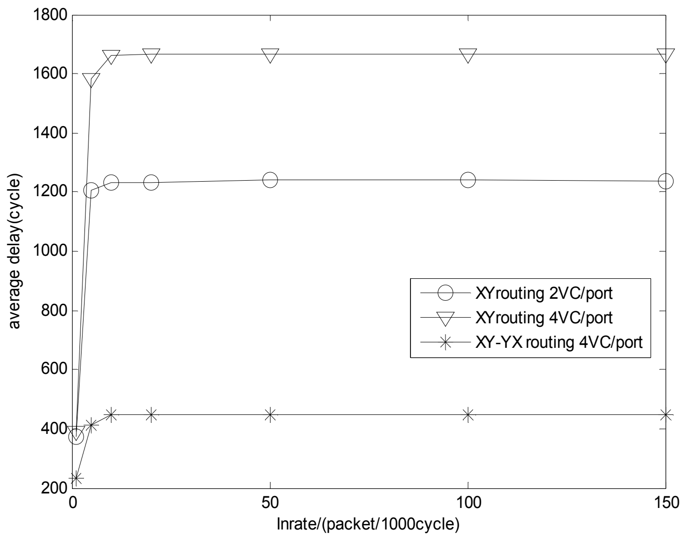


Fig. 8(a). The delays in uniform traffic scenario for traditional NoC and XY-YX dual subnets NoC

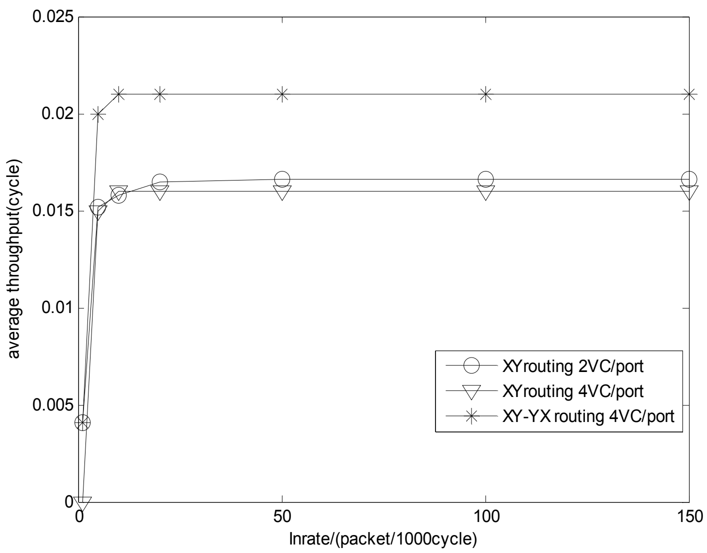


Fig.8(b). The throughputs in uniform traffic scenario for traditional NoC and XY-YX dual subnets NoC

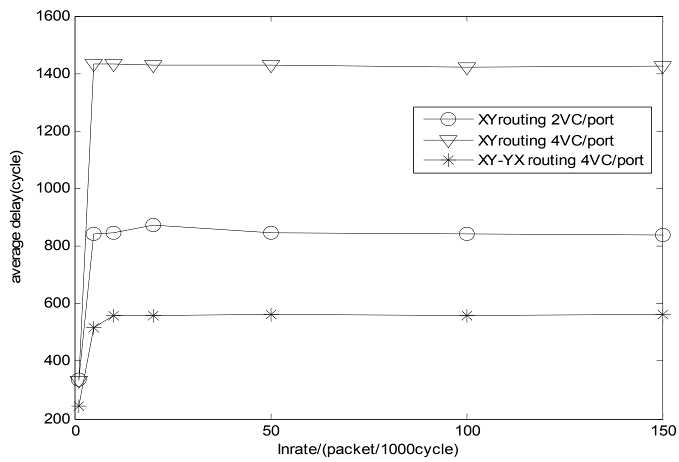


Fig. 9(a). The delays in hot-spot traffic scenario for traditional NoC and XY-YX dual subnets NoC

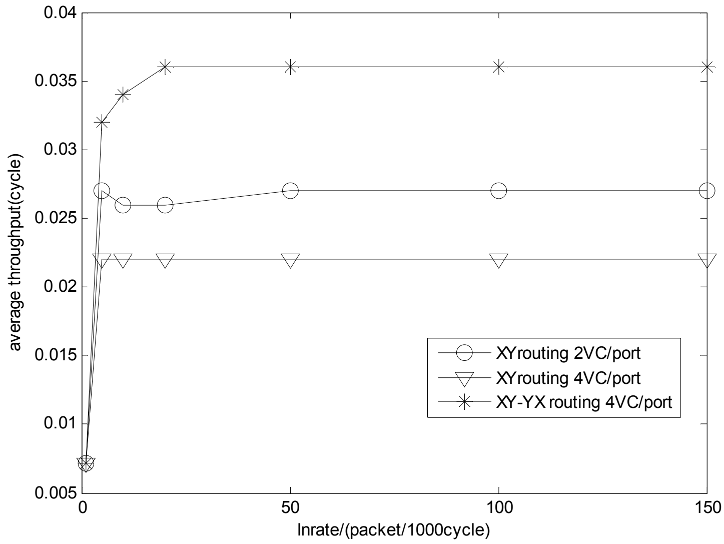


Fig.9(b). The throughput in hot-spot traffic scenario for traditional NoC and XY-YX dual subnets NoC

We calculate the delay and throughput at the interface between NI and local port in router. With the increase of injection rate, average packet delay of on-chip networks is growing until the network becomes saturated and propagation delay reaches its peak. This is due to the fact that NI tends to avoid network congestion. When the traffic flow from NI to router buffer approaches the upper bound, NI will automatically slow down its injection rate.

The delay and throughput performance is shown in Fig. 7 Fig.8 and Fig.9 respectively, when the packet size is 64. Fig. 7a and Fig. 7b. show the comparison of the delay and throughput in the extreme case in which the X direction is seriously blocked by the packet from the sending node which have the same y coordinate position. The XY-YX routing in dual subnets shortens the delay and increases the throughput significantly.

Fig. 8 and Fig. 9 show the performance of uniform traffic mode and hot-spot traffic mode, respectively. In both figures, Fig. a is for delay performance comparison, and Fig. b shows the throughput performance. From all these figures, we can see the XY-YX routing in dual subnets has a great advantage in all the scenarios.

The proposed algorithm greatly improves throughput and transmission delay at the cost of moderate increase of bandwidth. The extra bandwidth is worthy, especially in the scenario where short delay and high throughput are required.

4. Conclusion

In this paper, we proposed a real-time algorithm for dual subnets NoC. This XY-YX routing algorithm in dual subnet greatly improves the average transmission delay and throughput of NoC by dispatching packets into different directions to avoid potential congestion.

5. References

[1] Manho Kim , Daewook Kim , Gerald E Sobelman. Network on chip quality of service through multi protocol label switching[C]/ / IEEE International Symposium on Circuits and Systems. Island of KOS , 2006 : 4 - 11

[2] Axel Jantsch , Hannu Tenhunen. Network on chip [M] .Russia : Academic Publishers , 2003.

[3] Hu Jingcao, Ogras U Y, Marculescu R., “System Level Buffer Allocation for Application Specific Networks On-chip Router Design,” IEEE Transactions on Computer Aided Design of Integrated Circuit s and System, 2006 , 25 (3): 2919-2933.

[4] Vassos Soteriou, Rohit Sunkam Ramanujam,etc., “High Throughput Distributed Shared Buffer NoC Router,” IEEE Computer Architecture Letters, vol. 8, no. 1, January-June 2009:21-24.

[5] Vestias M.,Neto H., “Area and Performance Optimization of a Generic Network-on-Chip Architecture,” Symposium on Integrated Circuits and Systems Design, SBCCI’06, 2006:68-73.

[6] L EE J . Hardware/ software deadlock avoidance for multi- processor multiresource system-on-chip [D] . Atlanta ,GA : School of ECE , Georgia Institute of Technology ,2004.

[7] Jerraya A A , Tenhunen H , Wolf W. Introduction : multi-processor systems-on-chips[J] . IEEE Computer, 2005 ,38 (7) :36 - 40.

[8] Z. Li, X. Ling, J. Hu, “A Novel Network-on-Chip Simulation Framework for Parallel Software-Defined Radio,". Presented at the International Workshop on Software Radio Technology 2008, Beijing, China.

[9] J. Kreku, M. Hoppari, and T. Kestilä, “Application-platform performance modeling and evaluation,” Specification, Verification and Design Languages, 2008. FDL 2008. Forum on, pp. 43-48, Sept. 2008.

[10] Fangfa FU, Siyue Sun, Junjie Song,“A NoC Performance Evaluation Platform Supporting Designs at Multiple Levels of Abstraction,” 978-1-4244-2800-7/09 ©2009 IEEE