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The Combinational Test Generation Algorithm Based on Three-valued Neural Networks

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Abstract. With the growth in size and complexity of integrated circuits, test generation for them is becoming increasingly difficult, so it is important to find new and effective digital integrated circuit test generation algorithm. In order to improve the quality of combinational test generation, a combinational circuits test generation algorithm based three-valued neural networks [1] is proposed in this paper. This algorithm does not need propagation and backtracks, but represents the combinational circuits as a bidirectional network of neurons using the three-valued neural networks, and constructs the energy function for the network. The application of three-valued neural works may reduce research space and avoid many wasteful assignments, improve the efficiency of combinational test generation. A genetic algorithm was used to find the global minimal as the test vectors. So the problem of the combinational test generation was formulated to an optimization problem. The experimental results on some standard circuits demonstrate that the algorithm have high fault coverage and short test time.

Keywords: Three-valued neural networks;test generation algorithm; genetic algorithm; energy function

1. Introduction

With the development of the microelectronic technique, the scale of the integrated circuits becomes more and more large, the structure becomes more and more complex, and the test generation for integrated circuits is becoming increasingly difficult and time consuming. The traditional test generation algorithms are inefficient for the integrated circuits now. Consequently, new and effective algorithms are imperative research subjects today. Considering the neural networks' successful application in optimization, many scientists connected generation problems with neural networks and gained some achievement. But these algorithms are all based on two-valued neural networks [2], the test time is long and the fault coverage is not very high. Three-valued neural networks proposed by Fujiwara are used to the combinational test generation and test generation algorithm based on three-valued neural networks for combinational circuits is proposed in the paper. Representing digital circuits by three-valued neural networks may reduce research space and avoid many wasteful assignments. So three-valued neural networks' application in combinational test generation may reduce test time and improve test efficiency. Genetic algorithm was used to find the test vectors at last. The experiments results demonstrate that the algorithm have high fault coverage and short test time.

2. Three-valued Neural Networks

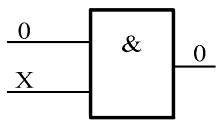

Figure 1. Two-input AND gate

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Every net (signal line) in the circuit can be represented by a neuron and the value on the net is the activated value of the neuron. The activated value can only be 0 or 1 in the Hopfield neural networks, so it is called two-valued neural networks. Japanese scientist Fujiwara improved the Hopfield neural networks and proposed three-valued neural networks. The neurons' activated values can be 0、1 and X, where X denotes don't care in three-valued neural networks. Considering the two-input AND gate in Figure 1, if we have to set the value 0 on the output of the gate, and search with values only from 0 or 1, we have to select one from 00,01 or 10 as the input of gate, and search with values from the set{0,1,x}, we can select one from 0x or x0, which reduces the search space. The energy function for three-valued neural networks is defined by the form:

$$E=-\frac{1}{2}\sum_{i=1}^{N}\sum_{j=1}^{N}T_{ij}V_iV_j-\sum_{i=1}^{N}I_iV_i-\sum_{i=1}^{N}\sum_{j=1}^{N}W_{ij}V_i\left(1-V_i\right)V_j\left(1-V_j\right)+K$$

where N is the number of neurons in the neural networks, Tij is the weight associated with the link between neurons i and j, V_i is the state value of neuron i, I_i is the internal parameter of neuron i, W_{ij} is the weight associated with the link between neurons i and j which is effective only when V_i and V_j are both X, and K is a constant. The activated values of neurons are 0,1 and x. We assume $T_{ij}=T_{ji}$, $W_{ij}=W_{ji}$ and $T_{ii}=W_{ii}=0$.

Three-valued neural networks can represent an arbitrary basic gate circuit and the value on the net is the activated value (0, 1 or x) of the neurons. The basic gate circuit is realized by specifying the matrices of weights $T=[T_{ij}]$ and $W=[W_{ij}]$ and vector $I=[I_i]$. After T,W and I are determined the energy function can be obtained for the basic logic circuit.Wherever Times is specified, Times Roman or Times New Roman may be used. If neither is available on your word processor, please use the font closest in appearance to Times. Avoid using bit-mapped fonts if possible. True-Type 1 or Open Type fonts are preferred. Please embed symbol fonts, as well, for math, etc.

3. Representing Combinational Circuit with Three-valued Neural Networks

The states that satisfy the circuit's function are called consistent states; other states that don't satisfy the circuit's function are called inconsistent states. The energy function has global minima only at the neuron states consistent with the function of the circuit. In this paper, the energy function's value is 0 for all consistent state and energy function's value >0 for all inconsistent state. So the transfer character of the circuit can be indicated by energy function. Combinational circuits are composed of basic gate circuits; so combinational circuit's three-valued neural networks can be gained by using gate circuit's three-valued neural networks. The method is following: (1) Connect the neurons corresponding to the input net of the same gate; connect the neurons corresponding to the output net of the same gate. (2) Merge the three-valued neural networks of different gates to a three-valued neural networks of combinational circuit, merge the same neurons to one neuron, add the corresponding states values, add the corresponding weight values, obtain the new state values and weight values. The energy function of the combinational circuit is the addition of all the gate circuits' energy function. The neurons' states are consistent states for the combinational circuit when the energy functions of all the gate circuits are all zero. For example, Figure2 is a simple combinational circuit; Figure3(a) is the three-valued neural networks of AND gate G_1; Figure3(b) is the three-valued neural networks of AND gate G_2; Figure3(c) is the three-valued neural networks of the simple combinational circuit.

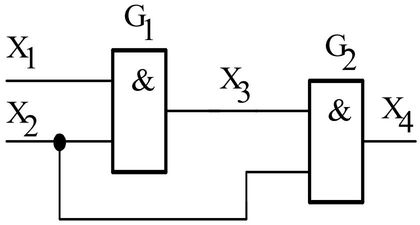

Figure 2. Simple combinational circuit

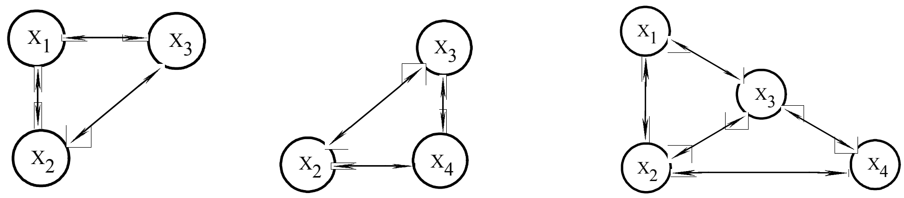

Figure 3. (a) Three-valued neural of G1. (b)Three-valued neural of G2 Figure 3. (c)Three-valued neural networks of circuit

4. Constructing the Constraint Network

There is a fault in a net of the combinational circuit, if there are input vectors that make the output of the faulty circuit differ from the output of the good circuit, and then these input vectors are test vectors for the fault of the circuit[3]. The constraint network[4] is the network that the output of the faulty circuit differs from the output of the good circuit when the test vectors are inputted to the network. The constraint network is needed to be constructed for combinational test generation algorithm based three-valued neural networks. The constraint network is constructed by joining the good circuit and a faulty circuit in such a manner that the primary inputs of the two circuits are connected directly and that the primary outputs are connected through an output interface. For single-output circuit, the interface is a not gate(Figure4). For m outputs circuit, the interface is composed of m two-input XOR gate and a OR gate, and the output of OR gate is 1 (Figure5).

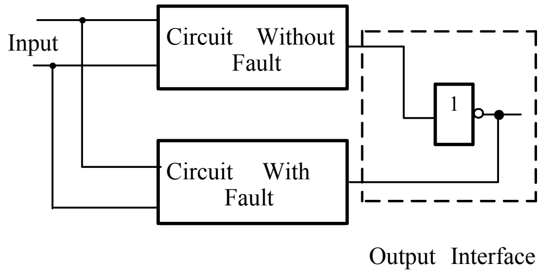

Figure 4. Constraint networks for single-output circuit

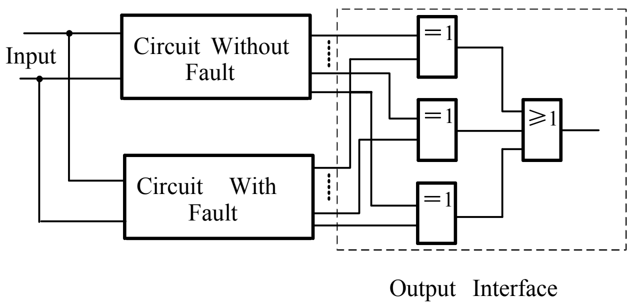

Figure 5. Constraint networks for m-output circuit

So the test vectors are consistent states for the constraint network and the energy function of the constraint network is zero at that time. In this way, combinational test generation problem can be formulated to find the minimum of energy function of the constraint network. It means the vector make the energy function's value 0 is the test vector for the fault.

5. The Algorithm's Realizing

After the circuit is represented with three-valued neural network, combinational test generation problem can be formulated to find the minimum of energy function of the constraint network. Generic algorithm is used to find the test vectors for the fault in this paper. Defining the scale of population N, the individuals in the population are x_i (i=1,2…N). The individual's fitness function is defined: $f(x) = 1/(1+E(x))$. E(x) is energy function of the constraint network. The value of f(x) is from 0 to 1. The value of $f(x_i)$ is bigger, the performance of x_i is better, and the individual x_i that make $f(x_i)$ 1 is a test vector for the given fault. Generic algorithm is constructed according to the organic evolution theory, it use selection、reproduction、crossover and mutation to provide global search and robust search [5], and it is often used to find a best global solution for the given problem. The detailed algorithm is following：

A. Define the scale of population N, the crossover rate PC, the mutation rate Pm; initiate the population.

B. Compute the individual's fitness function $f(x_i)$.

C. Find the individuals whose fitness function's value is biggest and smallest.

D. Replace the individual whose fitness function's value is smallest with the individual whose fitness function's value biggest.

E. Select two individuals according to the roulette wheel's rule, crossover according to PC, generate new individual.

F. Mutate the individual according to Pm, generate new individual.

G. If the test vector is found, the algorithm ends; else change (*B*).

The main program and subprogram on some ISCAS85 benchmark circuits' experiments are following:

```
/***save the test vectors******/
unsigned char vector[32*chromsize];
static int count=0;
void save_vector()
{ int i,j;
for(i=0;i<popsize;i++){
if(oldpop[i].fitness==0){
for(j=0;j<chromsize;j++){
vector[count*chromsize+j]=oldpop[i].chrom[j];
}
count++;
}
}
}
/***coding and fitness function**********/
void objfunc(struct individual *critter)
{ ...
critter->fitness=fitness function ;//compute the fitness function
...
}
void main()
{struct individual *temp;
initialize(); // initiate the population
for(gen=0;gen<maxgen;gen++){
save_vector();//save the test vectors for the fault
generation(); //generate new population
report(); // report new generation's statistical information
temp=oldpop;
oldpop=newpop; //refresh current generation with new generation
}
}
```

6. The Results of Experiments

Experiments were done for some ISCAS85 benchmark circuits on the Pentium4 computer(inner memory 256M), language C was used to write programs according to the algorithm of this paper and the algorithm based on two-valued neural networks. TABLE I are the results of experiments. From the results, we can know the algorithm of this paper have high fault coverage and short test time.

Table 1 The results of experiments

Circuit		C17	C432	C499
Faults Number		22	520	750
The Algorithm In This Paper	Faults Number Can Be Tested	22	515	745
	Average Test Time For Fault	0.018s	0.017s	0.017s
	Fault Coverage	100%	99%	99.3%
The Algorithm Based On Two-valued Neural Networks	Faults Number Can Be Tested	21	508	740
	Average Test Time For Fault	0.018s	0.021s	0.022s
	Fault Coverage	95.5%	98%	99%

7. Conclusion

Three-valued neural networks was used to combinational test generation in this paper, the application of three-valued neural networks may reduce research space and avoid many wasteful assignments, improve the efficiency of combinational test generation. The results of experiments demonstrate that the algorithm comparing with the algorithm based on two-valued neural networks have high fault coverage and short test time.

8. References

[1] Hideo FUJIWARA .Three-Valued Neural Networks for Test Generation. Proc.of 20th Fault-Tolerant Computing Symposium.1990.66～67

[2] S.T.Chakrdhar,M.L.Bushnell,V.D.Agrawal.Toward Massively Parallel Automatic Test Generation.IEEE Trans.Computer-Aided Design.1990,（9）：981～993

[3] Xue Jian Bin,Li Zhi.The Application of Neural Networks in the Simulation-based Test Generation Algorithm for Hybrid Circuits. Journal of Circuits and Systems.2001,6(4):109～110

[4] Liu Xiao Dong,Sun Shen He.The Combinational Test Generation Algorithm Based on Neural Networks. Journal of Harbin Institute of Technology.2002,34(2):256～257

[5] Chen Zhao Yang,Ding Ming Yue.A Robust Algorithm for Test Generation Based on Neural Network.Journal of Huazhong University of Science and Technology.1999,27(9):90～91