

Design and Optimization on the Interior DAC of SAR ADC

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Abstract. DAC is an important module within the SAR ADC, innovation design on DAC structure to ensure the accuracy of components is the key component to improve the performance of SAR ADC. Based on the comprehensive analysis on some kinds of DAC structures used in SAR ADC, the traditional structure of the resistance and capacitance structures was optimized and two innovative design methods were proposed in this paper for smaller chip area and higher accuracy, one is based on the non-lumped capacitors array, the other one is based on the capacitor compensation.

Keywords: SAR, ADC, DAC, C-R hybrid.

1. Introduction

Successive Approximation Register Analog to Digital Converter (SAR ADC) compares the input voltage and output voltage of an N-bit digital to analog converter (DAC) with only one comparator. The output voltage of DAC is used as a reference voltage; SAR ADC can get the final conversion result through a total of N times comparison. SAR ADC has moderate accuracy and moderate speed. It could achieve smaller chip area and low power consumption with CMOS technology. It is easy to implement multiplexing conversion and has comprehensive advantages in accuracy, speed, power and cost. SAR ADC is widely used in industrial control, medical instrumentation, microprocessor-assisted analog-digital conversion interfaces and other fields. SAR ADC linearity is mainly limited by the linearity of built-in DAC, the structure of DAC and the match precision of devices are the decision factors for ADC's performance. Therefore, it is the key component to ensure the performance of SAR ADC that design a DAC with considerable accuracy for the overall system. Based on the in-depth analysis about built-in DAC of SAR ADC, some modified D/A structures are proposed in this paper.

2. Structural Analysis on Interinal DAC Of SAR ADC

2.1. Traditional DAC with voltage scaling

Fig.1 shows the traditional structure with voltage scaling;

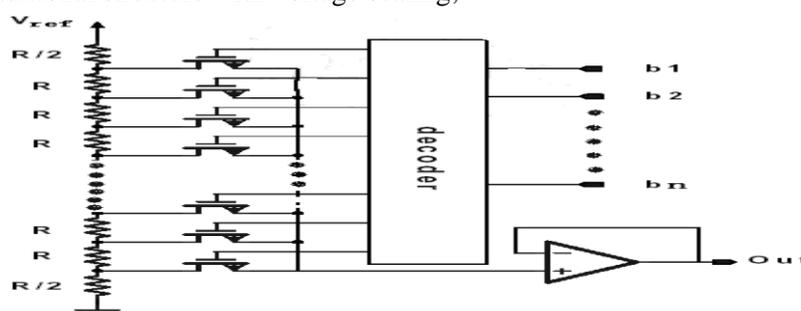


Fig. 1: DAC with voltage scaling

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It usually uses the series resistors that linked between VREF and ground to obtain the selective voltage. As for N-bit converter, it requires a series of resistors with equivalent resistance^[1].

$$V_{out} = V_{REF} * \frac{1}{2^{n+1}} (b_n * 2^n + \dots + b_2 * 2^2 + b_1 * 2^1 + 1) \quad (1)$$

The structure of DAC voltage scaling is very regular and suitable for CMOS technology. Since the voltage of each tap is not less than the following taps, thus ensuring its monotonicity. However, this kind of DAC needs larger area and the parasitic capacitance of each internal node will affect the conversion rate of converter, while it has high precision requirements for the resistor string. A little error in high-weight resistance will cause several bits error in the low bits. The worst differential nonlinearity (DNL) is equal to the results that difference between the actual step size and the ideal step size is normalized for the ideal step size. Therefore, DNL can be expressed as bellow:

$$DNL = \frac{v_{step}(actual) - v_{step}(ideal)}{v_{step}(ideal)} = \frac{(R \pm \Delta R)V_{REF}}{2^N R} - 1 = \frac{\pm \Delta R}{R} LSBs \quad (2)$$

For 12-bit DAC, to make the DNL < 1LSB, then

$$\frac{\pm \Delta R}{R} < 1LSB \text{ }^{SO}, \quad \frac{\Delta R}{R} < \frac{1}{4096}$$

The error of SAR ADC is the largest at the 2n points, such as the 128, 256, 1024 and other points. The conversion voltage of 1024 is even smaller than the voltage value of 1023. This is reason that DNL value of lots of SAR type devices based on this structure are more than 1. This structure is difficult to achieve high accuracy in the process,. However, this kind of SAR ADC's INL is very small, because the error of weight resistance does not accumulate. In addition, the ADC based on this structure requires an additional capacitance to sample the input signal during the conversion process; it has a greater impact on the chip area and performance.

2.2. Traditional D/A converter with charge redistribution

Compared with resistor divider type, DAC based on weight capacitor is improved largely on the production process, power and conversion accuracy. Its several advantages as shown below: firstly, the steady-state value of output voltage VDAC seems unaffected by switch resistance and resistance of reference voltage source, thereby reducing the request of the switching circuit and reference voltage source. Secondly, the capacitors array does not consume power during steady state, it helps to reduce the static power Consumption; thirdly, the accuracy of output voltage is only related to the capacity ratio of each capacitor instead of the absolute value of their independent capacity. Although the DAC with capacitors array has many advantages, it is difficult to make the DNL < 1LSB for high resolution. Fig.2 is 4-bit D/A^[1]:

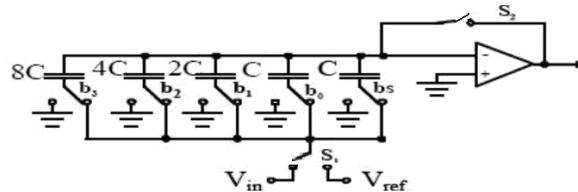


Fig. 2: 4-bit D/A based on charge redistribution

For the above circuit,

$$V_{out} = V_{REF} (b_N 2^{-1} + b_{N-1} 2^{-2} + b_{N-2} 2^{-3} + \dots) \quad (3)$$

assuming capacitance tolerance is ΔC ,

$$C_{max} = C + \Delta C, \quad C_{min} = C - \Delta C$$

Only the bit-i capacitor is connected to Vref, the actual worst output of the bit-i is:

$$V_{out}(actual) = \frac{(C \pm \Delta C) 2^{N-i}}{2^N C} * V_{REF} = \left(\frac{2^N}{2^i} \pm \frac{2^N \Delta C}{2^i C} \right) LSB \quad (4)$$

$$V_{out}(ideal) = \frac{2^{N-i} C}{2^N C} V_{ref} = \frac{2^N}{2^i} LSB \quad (5)$$

Because when the MSB changes, the worst DNL will take place, we can get the following results by the formula (1):

$$DNL = \frac{v_{step}(worst)}{v_{step}(idea)} - 1 = \frac{v_{out}(10000.....) - v_{out}(01111.....)}{LSB} - 1$$

$$= \frac{\frac{2^{N-1}(C + \Delta C)V_{REF}}{C_{total}} - \frac{(2^{N-1}-1)(C - \Delta C)V_{REF}}{C_{total}}}{V_{REF}} - 1 = (2^N - 1) \frac{\Delta C}{C} LSB \quad (6)$$

In view of a 12-bit DAC, to make the DNL < 1LSB, then $(2^N - 1) \frac{\Delta C}{C} < 1$

Thus: $\frac{\Delta C}{C} < \frac{1}{2^{12}-1} = 0.024\%$

Seen from the above analysis, If the DAC use the above structure which based on charge redistribution, and N = 12, it shows that the ratio of MSB and LSB capacitance is 2048:1 in extreme cases. The accuracy of the DAC is related to the ratio of capacitance, so the main disadvantage of DAC with capacitor array is that capacity of each capacitor vary widely when the input digital bits is numerous. It will not only account for a large area of integration, , but also the capacitance matching accuracy must be better for higher resolution, this precise capacitance matching requirements will bring some difficulties for the design and technology, so it will directly affect the INL and DNL of the converter. In addition, the capacitor's discharge time will reduce the accuracy of the conversion circuit.

In order to trade-off between the resolution and the ratio of the maximum and minimum components, two 6-bit sub- DACs based on charge scaling were usually used to combine into a 12-bit charge scaling DAC, but its performance is sensitive to the parasitic capacitance. The DAC with two 6-bit charge-scaling sub-DACs is shown in Fig.3:

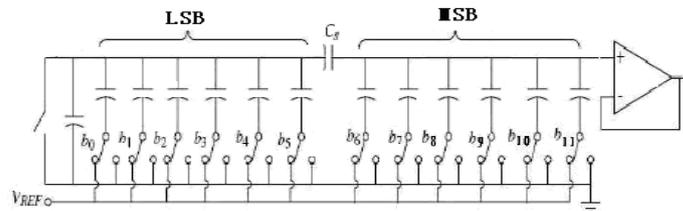


Fig. 3: 12-bit D/A consisted of two 6-bit charge scaling sub-DACs

The Cs is coupling capacitor; the value of Cs could be calculated by the following formula:

$$C = \frac{1}{\frac{1}{Cs} + \frac{1}{64C}}$$

$$\frac{1}{Cs} = \frac{1}{C} - \frac{1}{64C} = \frac{63}{64C}$$

Taking into account the capacitance matching and accuracy, this capacitor CS can be composed of the scaling network with some capacitance units, which is shown as Fig.4:

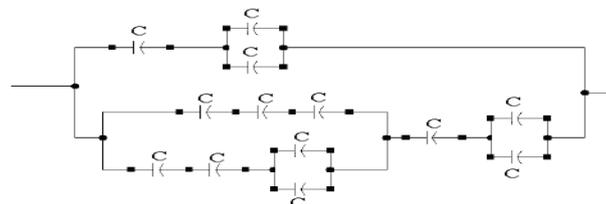


Fig. 4: Network structure of capacitor Cs

The 12-bit D / A converter is composed of the two 6-bit low-precision charge scaling sub-DACs through the coupling capacitor Cs. The capacitance ratio between MSB bit and LSB bit will reduce in a certain extent, but the design precision value of the coupling capacitor Cs is the key to the success of this kind of coupling structure, the weight relationship between each bit can be ensured only with selection of the correct and accurate coupling capacitance. Therefore, the parasitic capacitance in the layout design will bring greater effects for the precision of coupling capacitance. So in order to reduce the impact of parasitic capacitance,

usually increasing the capacitance value of the low weight bit, which also increases the capacity of the coupling capacitor's value, so that would cause to the bigger chip area, while bring the extremely high demand to the back-end layout design.

3. Design and Optimization of D/A with Resistor-Capacitor Hybrid

Based on the above analysis, if only using a calibration method, with the increasingly high resolution DAC, the ratio of MSB and LSB components value also will increase, matching accuracy of the components decreases with the ratio increasing between the largest and the smallest components, it is difficult to achieve high-precision. Therefore, R-C hybrid DAC with the resistor string and capacitor arrays is usually adopted in SAR DAC, which is combination of two different scaling types DAC, MSB DAC uses charge scaling, while the K-bit LSB sub-DAC uses voltage scaling. This advantage of this structure is that the MSB DAC is consisted of capacitors, which have higher accuracy those resistors on the processing craft. The LSB DAC is form by resistors string, it is monotonous, and so it would not be non-monotonic on the overall performance. Here is an example of 12-bit SAR ADC, after a compromise considerations between size and accuracy, the M is usually taken as 5, while the K is taken as 7, as shown in Fig. 5.

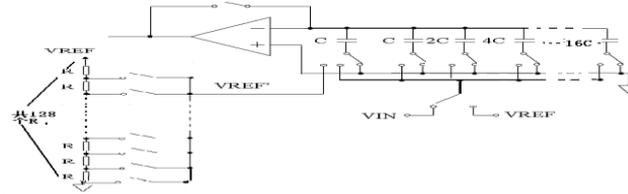


Fig. 5: Traditional Capacitor-Resistor hybrid D/A structure

For resistor-capacitor hybrid DAC architecture, DNL is calculated as:

$$DNL = DNL(R) + DNL(C) = \left[\frac{\Delta R}{R} + (2^N - 1) \frac{\Delta C}{C} \right] LSB \quad (7)$$

As expressed in e.q.(7), we can find that the tolerance of Capacitor is the main factor which affects DAC's DNL, the scale factor is about 2^N . Therefore, in order to get small DNL during the whole design, the capacitor structural Optimization must be proceeded to reduce the capacitance tolerance as far as possible.

3.1. Optimization of R-C hybrid DAC based On C-Array

In order to reduce the capacitance matching errors, an innovative C-carry architecture is discussed in the paper, aimed at the traditional lumped capacitors. The new capacitor array is composed of identical unit size capacitors, and no capacitors are lumped together.^[2] As an example, a 6-bit traditional SAR-ADC with C-R structure is used to illustrate the program's implementation method clearly, as is shown in Fig.6.

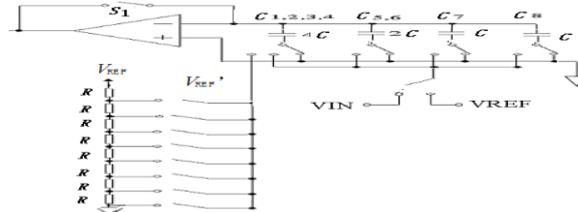


Fig. 6: 6-bit traditional lumped Capacitor carry structure

In fig.6, $C_1=C_2=C_3=C_4=C_5=C_6=C_7=C_8$, Comparison conversion process of SAR is based on the charge sharing. The working process is: when switch S1 is closed, the bottom plates of all capacitors are connected to the analog input to sample Vin; then S1 is disconnected, begin to the process of Successive Approximation, the bottom plates of C_1-C_7 are connected to V_{REF} or GND under the control of digital code 0 or 1, while C_8 is always connected to V_{REF} . (V_{REF}' is the voltage of output node of LSB sub-DAC) The voltage provided by the resistor string is determined by output node, so

$$V_{REF}' = \frac{1}{8} V_{REF} * M \quad (8)$$

As expressed in e.q. (8), M is the M th output node of the R-string from up to down. The value of M is from 0 to 7, so the C_8 can be equivalent to $1/8(M \cdot C)$, and its bottom plate is connected to V_{REF} . Now we adopt C_{eq} to show the total capacitance which is connected to V_{REF} , including the $1/8(M \cdot C)$, then

$$VDA = \frac{C_{eq}}{C_{total}} * V_{REF} \quad (9)$$

DNL errors are generated due to mismatch of the capacitors and monotonicity is not guaranteed. For example, if the output code is 001_111, $C_1, 2, 3, 4$, and $C_5, 6$ are connected to ground, C_7 is connected to V_{REF} , then additional capacitor C_8 is always connected to V_{REF} . At that time, $V_{REF}' = 7 / 8 * REF$, then the total equivalent capacitance $C_{eq} = C_7 + C_8 * (7 / 8)$; the next output code is 010_000, and $C_{eq} = C_5 + C_6$. Obviously, the mismatches between C_7-8 & C_5-6 in the layout design and manufacturing processes make DNL errors directly; it will affect the dynamic and static performance of IP core.

In view of the above error factor, the optimized SAR ADC with new capacitors array is shown as Fig.7:

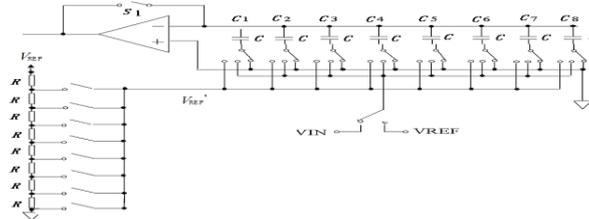


Fig. 7: Optimized capacitor carry structure

The main difference from the traditional C-R structure is: first, the capacitor array is composed of identical unit size capacitors, no capacitors are lumped together; second, Each unit capacitor can be connected to both V_{REF} and V_{REF}' . As for a 12-bit SAR ADC, according to the design method, we changed the capacitor array 16C: 8C: 4C: 2C: C: C in MSBS DAC into an array of non-lumped capacitance structure with 32 units capacitors. Every capacitor may be connected to V_{REF} or V_{REF}' . The improved C-R structure is shown as Fig.8.

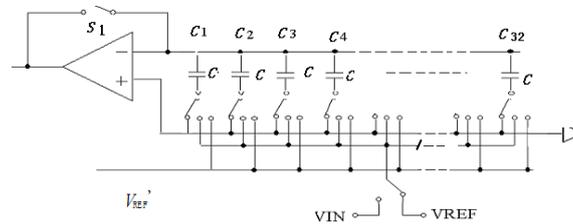


Fig. 8: Non-lumped capacitance structure

During the conversion process, the feedback switch is open, circuit starts conversion approaching when $D[11:0]$ is 100000000000, the front 16 units of capacitors are connected to V_{REF} at this time, then the 17th capacitor is connected to V_{REF}' , the other capacitors grounding. If the final comparison result is greater than 1, then the highest bit 1 is reserved. $D[11:0]$ turns into 110000000000, this front 24 capacitors are connected to V_{REF} , the 25th capacitor is connected to V_{REF}' , the other capacitors are connected to the ground; If the final comparison result is less than 1, $D[11:0]$ turns into 010000000000. Then the front eight unit capacitors are connected to V_{REF} , the ninth capacitor is connected to then V_{REF}' , the others are grounded, and so on. After the final conversion of the last bit is finished, the conversion is complete, and the N -bit digital word is available in the register.

The connected capacitors do not change for the each additional 1 LSB of output code under the control of the digital logic. The design provides a scheme to improve the DNL significantly in the C-R structure of SAR ADC, ensuring the monotonicity of the output codes. As a result, the SAR ADC gets better performances by using the new C-R structure.

3.2. Optimization of R-C hybrid DAC based on capacitor compensation

The design of the DAC uses the other new type of R-C hybrid DAC structure. It is different from the previous voltage scaling and charge scaling method combined a simple, but on two levels conducted by voltage scaling at the same resistor string to convert, then the conversion results of the two levels was increased in proportion by two capacitors in the way of charge redistribution, and ultimately realize the DAC conversion. This will help to improve accuracy and reduce chip area and cost savings.

Fig.9 shows the 12-bit resistor-capacitor hybrid DAC^[3]. The higher eight bits B [11:4] are converted through voltage scaling conversion type sub-DAC with resistors string; VDAC was its output signal. In addition, the lower four bits B [3:0] are converted by the lowest part of resistors string, the output is set to VLSB, and then the VDAC and the VLSB are scaled up by two capacitors. The conversion progress of DAC was finished ultimately. The resistors string is shown as Figure 9, 16 resistors string were connected together; there is an $R/2$ at the top and bottom of each resistors string, there are 15 R resistors in the middle. There are all $127-R$ resistors and two

$R/2$ at top and bottom of the resistors string. The decoder adopted two-step decode structure, the high eight D [11:4] controlled the two decoders and decided the output node voltage VDA of resistors string. However, VDA is equal to the conversion result of shifting D [11:0] to the right 4-bit. In addition, conversion result of low 4-bit is the output VLSB under the control of D [3:0]. Finally, VDA were increased scaling to 16 times based on capacitor compensation with the two capacitors $16C$: C .

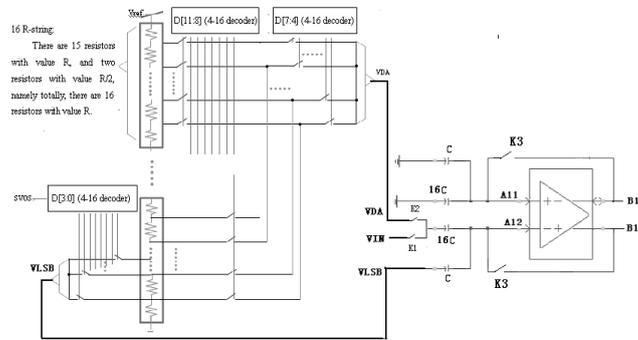


Fig. 9: Optimized D/A

VLSB and VDA were connected to the input nodes of comparator. Since the interior DAC is R-C based approach, sampling and holding circuits could be embed in the DAC. For analog input signal is single-ended, we use a quasi-differential comparator structure in order to reduce noise. Groups of dummy capacitors, which are identical to the sampling capacitors, are added to the inverting input terminal of comparator, and all the Dummy capacitors are grounded. This structure obtained both the advantages of differential structure and reduced the chip area in a certain extent, increased its cost effectiveness.

During the sampling, while switch K1 and K3 are on, K1 is off, analog input V_{in} is stored in node A11, in fact, it is the charge that is stored in capacitors. Then $SVOS=1$, VLSB is equal to the voltage of the ninth node under the control of signal SVOS. So

$$VLSB = \frac{VREF}{256} (8 + 0.5) \quad (10)$$

During the Conversion, K3 and feedback switch K1 are off, K2 is on, charge stored on the input capacitors remains unchanged, VA11 keeps the same value of sampling.

$$VDA = \frac{VREF}{256R} (NR - \frac{R}{2}) = \frac{VREF}{256} [2^{-4} \sum_{i=4}^{11} D_i 2^i + 0.5] \quad (11)$$

The value of VLSB' is decided by D[2:0] completely,

$$VLSB' = \frac{VREF}{256} [\sum_{i=0}^3 D_i 2^i + 0.5] \quad (12)$$

From e.q. (10), (11), (12), the difference between A11 and A12 of input nodes of comparator reached after analysis:

$$\begin{aligned}\Delta U &= V_{A12} - V_{A11} = 16 * (V_{DA} - V_{IN}) + (V_{LSB} - V_{LSB}) \\ &= 16 * [V_{IN} - \frac{V_{REF}}{4096} \sum_{i=0}^{11} D_i 2^i]\end{aligned}\tag{13}$$

If $\Delta U > 0$, then the output code of comparator is 1, otherwise output is 0.

4. Summary

The speed and resolution of SAR ADC is limited mainly by the built-in DAC's speed, resolution and linearity. Exact design of DAC is the focus and key to ensure the performance of SAR ADC. Based on the in-depth analysis about traditional R-C hybrid D/A converter, two modified D/A structures were proposed in this paper, one is based on the non-lumped capacitors array, the other one is based on the capacitor compensation. That innovative design could improve the accuracy of DAC further, reduce chip area of the DAC and will continue to promote the SAR architecture forward.

5. References

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