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The Physical Design of Long Time Delay-chip

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Abstract. Focused on off chip traditional RC delay circuit, this paper designed a digital delay circuit to implement on chip delay circuit. Based on HJ 0.18 um 1P3M technology, the timing closure design flow of Soc Encounter was adopted, including floor plan, timing-driven placement, static timing analysis and optimization, clock tree synthesis and timing-driven routing. The design have passed the DRC and LVS, and fully implemented.

Keywords: Physical design; Floorplan; Delay Circuit

1. Introduction

Delay circuit is a form of circuit module that is often used. RC circuit is easy to build, and the price is cheap, but its shortcoming is obvious. First the core of RC circuit is established by resistance and capacitance. But the problem of big capacitance integration has been difficult to get effective solution. The complex PLD device is programmed by other hardware description language. It which accelerates the product development process, and make the design of purely digital circuit be simple. Traditional sound and light control lamp is design by RC delay circuit. Its disadvantages have been show as the great power consumption, low reliability, big volume and so on. With integrated circuit of the widely used in daily life, we can imagine that if the integrated circuit design and traditional integrated circuit be used to design the digital delay circuit with EDA technology , it can easily be used to instead of traditional RC circuit. This chip adopt two-stage nested counters add comparator to achieve the purpose of the long time delay.

2. The long time delay chip front design

This chip mainly contains a 12 counter, a 12 comparator, 48 a counter, 48 a comparator and top design five modules.

After HDL levels code Design completed, on the basis of success in functional verification, through Synopsys Design Compiler, combined with the Compiler HJ180nm six-story metal craft, we compiled it into RTL code, then transforms RTL code into the door level nets table, and export the timing constraints documents that be required in the back-end Design. The Design Compiler of the chip is shown in Figure.1

3. The long time delay chip physical design

We begin the physical design of chip on the basis of door level nets table that exported by front design, realize of transformation that from the table to GDS Ⅱ level nets. We use Enounter platform of Cadence to design the physical chip, adopting timing convergent design process, including layout planning, layout, clock synthesis timing optimization, routing steps, eventually derived GDS Ⅱ documents[1]. The physical design process is shown as the Figure.2.

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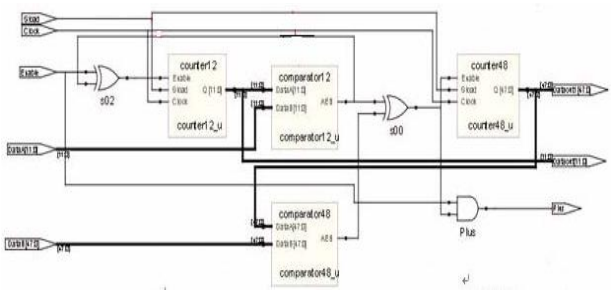

Figure 1. DC of the long time delay-chip

3.1. Layout planning

The long time delay integrated circuit chips contain 126 functions I/O Pad. 24 power I/O Pad. The type of chips limited is pad limited. It is perfect that the design of the long time delay chip tube feet roughly be distributed around the chip equally.When planning for pad, considering the clock signal is very important in the chip.We provide the special protection for input clock Pad, namely select pad with schimidt Special hysteresis effect, and both sides placed Pad had power to Pad (VSS Pad). That can reduce other signal to the clock signalInterference, makes the input of the chip clock is an edge steep square Wave.Maintaining the Integrity of the Specifications

3.2. Power planning

For 180nm and below deep sub-micron DFM back-end physical design, wire are more important than gate delay, including power distribution network, in all of the interconnect the impedance characteristics will show unusually obvious .Chips of I/O voltage is 1.8V. Its Power and grounding lines are bring in the chip’s internal by the pads around the chip, Power Ring is constructed by two wide line metal layer (M5 and M6) around the core of the chip, we design the longitudinal power strips throughout chip every certain spacing, combined with the lateral Power rail and finally formed an fluctuation two layer cross-cross of Power grid. Power strips is made of senior Metal (Metal 6 ~ Metal 4), because the thickness of top Metal is enough to bear the bigger current density, small resistance and parasitic capacitances, high reliability [2].

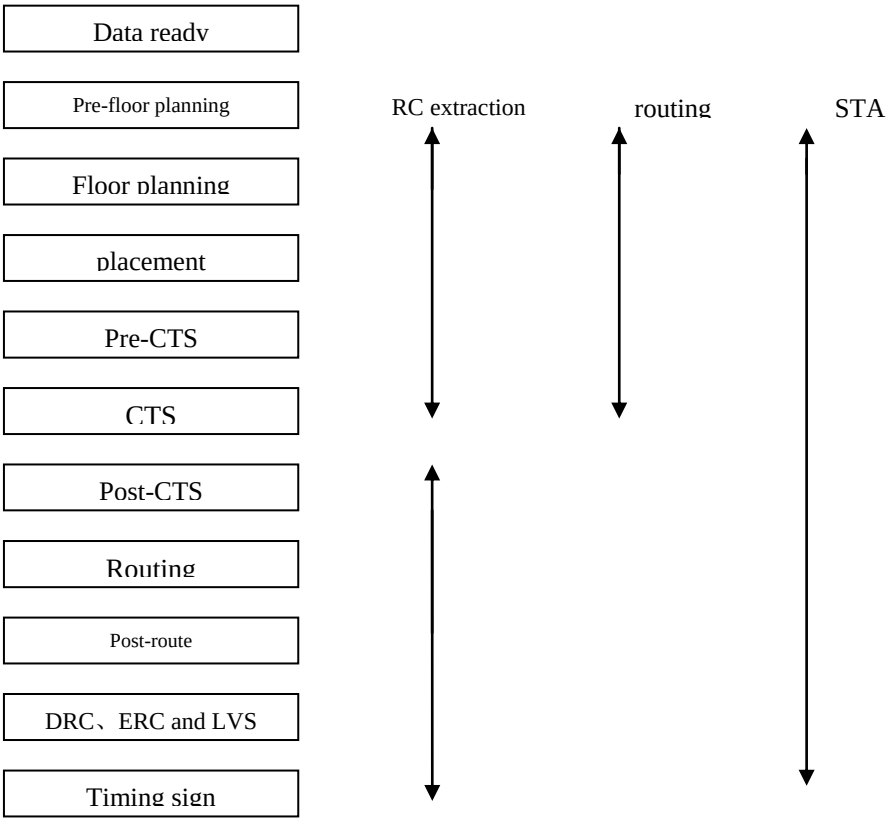

Figure 2. Physical design process

When power grids are be constructed, there are contradictions between the number of power and routing resources .If power strips are too much and close, it will need too much Via in order to connect the first level metal with the 6th layers of metal. That will take up too much routing resources and easy to cause the routing behind doesn't go through. Our solution is adding narrow the layer metal 4 power strips below the power strip of metal 6, then let the first level metal connect to the layer 4 metals directly. It released Metal 4 and 5 resources. Facts prove that adopts appear wiring congestion (congestion).Besides, use this method, is successfully passed the wiring. Moreover, it scheme has been confirmed by IR Drop verification, guarantee the voltage Drop the scope of the permit.

3.3. Timing Driven planning:

On the basis of chips for layout, we adopt Timing Driven way to put standard units. The tool will automatically search the critical path in the design, balance the constraints of setup time and keep routing space for these critical path, enhance key signal wire Jacobson connectivity.

3.4. Clock tree synthesis

Achieving results of the clock signal in physical design has been aptly called clock tree. Clock tree can reduce due to clock skew due to the different path length. It will insert special clock buffers at the begin of t or in the end of he clock path .it will balance the clock phases difference between root and leaf, reduces the clock skew and transmission delay[3]. Clock tree timing constraints basically has: Min Delay, Max Delay, Max Skew and Max transition. Due to The self Heat on the actual clock circuit, we should make the clock tree the biggest rise time as small as possible.

Since the chips with larger area, the distance of the memory and standard unit are big, therefore in the attachment capacitance larger integrated circuit layout we advance the line joining comprehensive constraint value of capacitance. According to such constraints, the comprehensive tools strength the corresponding line driver ability, to make the result more close to the real layout routing results.

On the whole circuit layout routing of analysis results, we found that the critical path of maximum delay is relatively easy enough, but many attachment length are longer than expected, which make the transition of the line a too big. Due to the comprehensive tools and layout tools interface problems, cabling connections in the layout of the length of the optimization effect is limited, thus in logic synthesis and optimization process we select some drivers had small unit, and ability makes the problems obviously improved.

We synthesis 4 clocks in proper order, but synthesis the most important clock at last. This is because the clock ahead synthesis may be affected by the clock buffers which inserted do (buffer) behind. This design clock tree in topology is used on H clock tree. Figure 3 shows the CTS of the chip.

3.5. static timing analysis and optimization

Before clock tree synthesis, we must resolve Setup violations, we needs static timing analysis and optimization after the layout [4]. Parameters extraction of Interconnect RC and delay calculation is the prophase work of static timing analysis. the timing analysis before Clock tree synthesis is Setup, namely the clock function frontier (or along the) before the arrival of synchronous input signals must be stable during that time to make any signal not lost, If there are setup violations in design of the Setup, timing optimization will be needed. After Clock tree synthesis the time-series analysis type is Setup and Hold. Hold requires synchronous input signals must be stable for a period of time to make any signal can be successfully latch clock function front edge(or end edge)arrive. If there are timing violation, timing optimization will be needed.

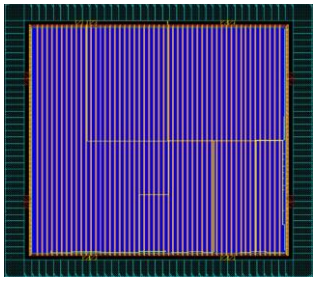

Figure 3. Layout of CTS

Timing analysis is needed after Detail routing. We use IPO(In place optimization) .for example, select and replace the logic unit that have different driving capability. Copy a logic unit in order to Shared load (Cloning); Add "buffer" (Buffering) or use the buffers to replace two inverters and so on.

3.6. Timing-driven routing.

Use Timing-driven routing. It will be consider such as each unit driving intensity and largest capacitor and maximum transmission delay, in order to ensure that timing violation as few as possible; Routing device in sequential critical path will try to avoid detour bypass to make attachment as soon as possible in the timing of the critical path [5].

This paper uses the timing driving global detailed routing make all timing analysis founded on the basic of attachment which get through delay through the RC parasitic parameters to extract, request all attachment the demands of meet timing constraint. Due to this design of 0.18 um manufacturing process and in routing stage we should also consider the signal integrity, we adopt the SI driving and limits parallel connection string length, and repair the cross-talk iterative. Layout of the Routing is shown as the Figure.4.

3.7. PAE Preventive repairing

The accumulation and instantly putout of charge, it can cause gate oxide layer damage, even with breakdown the gate oxide layer which caused chips failure. There are two ways to solve the antenna effect basically, one kind is to add the partial diode, make the gate oxide layer of area Unit area bigger. The second is to change the metal attachment, cut long underlying metal into a few short metals, make metal wire which connect gate oxide layer metal shorter. Thus the charge will be less accumulated [6]. Near the input MOS tube grid position We Placed reverse bias diode. It can effectively avoid PAE the happening of the problem. Figure.5 shows the example of inserting diode to solve antenna. The red circle marked is the diode unit inverting.

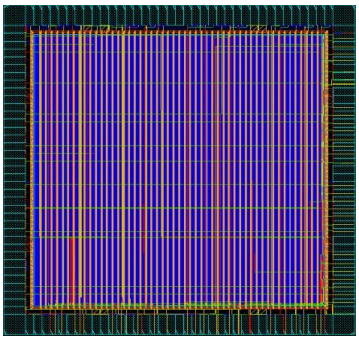

Figure 4. Routing

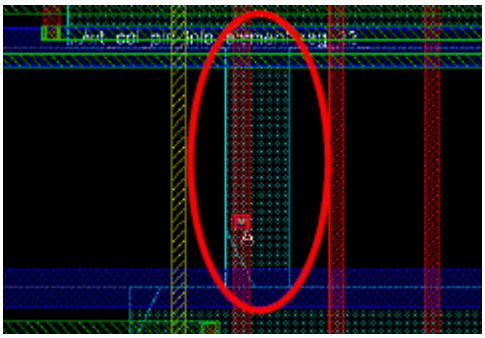

Figure 5. The example of inserting diode to solve antenna in this chip

3.8. Physics verification

The revised territory derived GDS II files, conduct DRC and LVS [7]. The design rule is that, according to manufacture technological level and considering other factors, the characteristic dimensions of devices as a benchmark, formulate a set of the minimum allowable value of graphic and relative size between graphics about the mask related layers. DRC is to inspect the size of graphic on the mask layers, and make sure there is no violation of regulations design rules. This mistakes that design DRC check for is i_2 ME2. It is because the distance between two Metal4s is too close. After locating the DRC wrong location, we find that it is cause by overlap of Via13 (Metal3 and Metal4 layer hole) and Via4, it lead tool calculates metal spacing according to hole width .Solution is to make the distance of via3 and via4 bigger, connect them by Metal4.

In DRC rules specified file there are a minimum width for 0.60 um in the first layer metal wire and wire. But the distance of wire and wire are less than 0.60 um in the layout which shown in the Figure.6. Because the width of signal wire is fixed, besides the metal wire may be altered. We correct the mistakes by changing the width of Fill metal line.

Before LVS check, we should tag each Pad's name using metal in the corresponding place of territory, and tag the name of power in the correct position. Addition, generate Spice nets list which is the form of CDL, and

plus the commands that contains HJ company I/O unit and the SPI files that used before generating the nets table of CDL. After the corresponding processing, design success through LVS check. The final layout is shown in Fig. 7.

The chip has totally 129 I/O pads, 128 nets, 7 cells, 172337 gates and the total area of which is 927737.0 um^2.

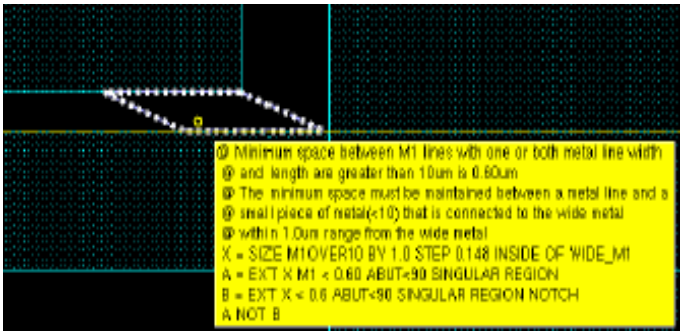

Figure 6. The mistake of min width

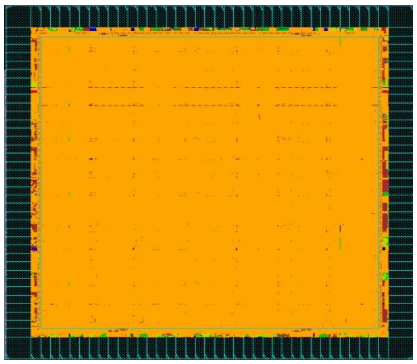

Figure 7. Final layout of the chip

4. Conclusion

This paper mainly studies physical design process of the long time-delay chip, design based on HJ 180 nm six layers of metal technology, using the SoC Encounter timing convergence process design. This design successfully implemented a digital delay circuit, which passed the LVS DRC, physical test and verification.

5. Acknowledgment

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