

# The Layout Design and Optimization of A Low Dropout Regulator

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**Abstract.** In various types of integrated circuits, the analog IC are more rely on the layout due to its operating state with a deep relation with the characteristics of analog device. Therefore, the design of optimized layout becomes more and more important .This paper presents several optimized layout design methods and the optimized LDO layout was designed using these proposed methods. The whole layout design of LDO regulator manually uses Cadence's Virtuoso and chartered 0.35um CMOS process.

**Keywords:** LDO; Layout Optimization; Analog IC; Cadence Virtuoso

## 1. Introduction

The scaling of feature size in VLSI circuits, both digital and analog, has been one of the strongest driving forces toward the rapid development of electronics technology. Layout is the process of specifying the physical placement of and interconnections between all of the devices in a circuit. The accomplished layout is used to generate the entire mask layers used for chip fabrication.

The IC layout design is assembled by using cell layouts from the cell library; this assembled IC design layout is ready for submission for fabrication. The target layout must be passed Design Rule Check (DRC) and Layout versus Schematic (LVS). Optionally, if desired, the designer may also undertake a SPICE-level simulation of the interconnected functional cells before and after the layout step.

Low Dropout regulator (LDO) is an analog chip and its function is providing stable output voltage when the input voltage fluctuations. Even if we input the same signals to LDO regulator, the output results from different layout also have some differences. Therefore, this requires us to optimize the layout to achieve more accuracy output results. In this paper , several optimized methods of design layout are proposed and use this approach a optimized LDO regulator layout was designed. This paper is organized as follows, section II presents some optimized design methods. In section III introduces the basic structure and operational principle of LDO, and the LDO regulator's circuits laid-out manually using Cadence's Virtuoso with multi-finger transistor structures and the used technology is chartered 0.35um CMOS process. Finally, conclusions are summarized in section IV.

## 2. Optimized methods of layout design

Design rules specify a minimum length and width of the device (as Fig.1 shows) Due to the signal we processed is an analog value, this requires us to ensure that the output signal cannot be distorted as well as the area of the layout be optimized. We have taken several effective methods as shown below which aims at the layout can be precisely matched with the designed schematic.

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		Width	2.50
12.1.2		Well to well spacing	
	12.1.2.1	Equi-potential wells or Different-potential wells	0.60
12.1.3		Overlap of Ncomp IN HVPW	3.60
12.1.4		Overlap of Pcomp well tap	0.20
12.1.5		Space to the edge of the scribe line	5.20
12.1.6		Space to DNWELL	5.00
12.1.7		Space to Nwell	3.00
12.1.8		Space to Ncomp in substrate/Pwell	4.0
12.1.9		Space to Pcomp well tap in substrate/P-well	1.5

Fig.1 Example of chartered 0.35um design rules

## 2.1. Multifinger Transistors

Wide transistors are usually "folded" so as to reduce both the S/D junction area and the gate resistance. A simple folded structure such as that in Fig.2 (a) may prove inadequate for very wide devices necessitating the use of multiple "fingers"[Fig.2 (b)]. As a rule of thumb, the width of each finger is chosen such that the resistance of the finger is less than the inverse transconductance associated with the finger .In low-noise applications, the gate resistance must be one-fifth to one-tenth of  $1/g_m$  .[1]

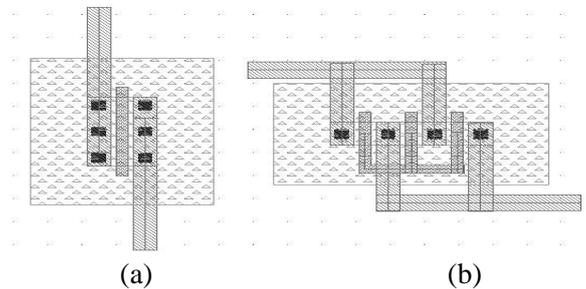


Fig.2 (a) Simple folding of a MOSFET, (b) Multiple fingers.

## 2.2. Symmetry

Symmetry must be applied to both the devices of interest and their surrounding environment. Symmetries in fully differential circuits introduce input referred offsets, thus limiting the minimum signal level that can be detected. While some mismatch is inevitable inadequate attention to symmetry in the layout may result in large offsets. Symmetry also suppresses the effect of common-mode noise and even-order nonlinearity.

Let us consider the differential pair of Fig.3 (a) as the starting point. If, as depicted in Fig.3 (b), the two transistors are laid out with different orientations, the matching greatly suffers because many steps in lithography and wafer processing behave differently along different axes. Thus, one of the configurations in Fig3(c) and Fig3(d) provides a more better solution.[1]

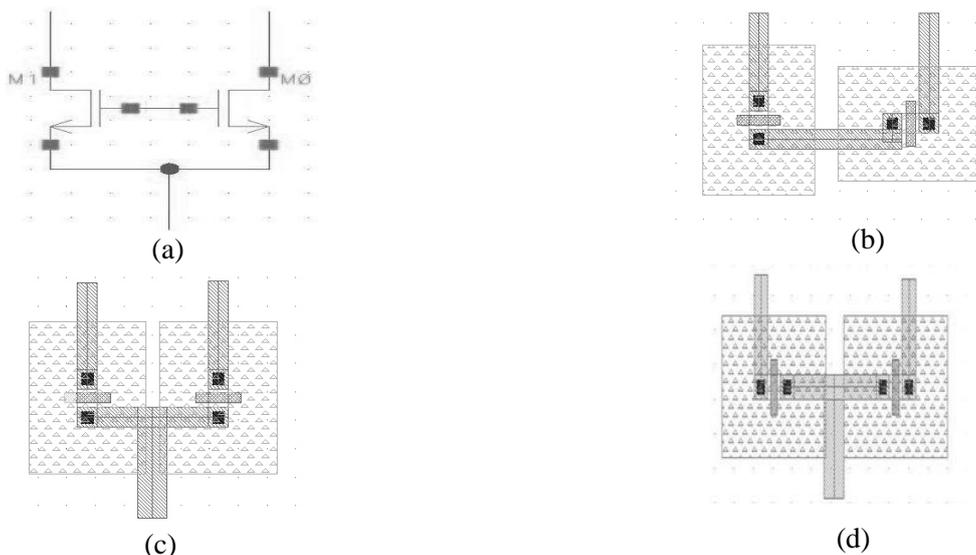


Fig.3 (a) Differential pair. (b) Layout of M0 and M1 with different orientations. (c) Layout with gate-aligned devices. (d) Layout with parallel-gate devices.

## 2.3. Resistors

Polysilicon resistors using a silicide block exhibit high linearity, low capacitance to the substrate, and relatively small mismatches. The linearity of these resistors in fact depends on their length, necessitating accurate measurement and modeling for high-precision applications [2].

As with other devices, the matching of polysilicon resistors is a function of their dimensions. For example, resistors having a length of 5 $\mu$ m and width of 3 $\mu$ m display typical mismatches on the order of 0.2%. Most of the symmetry rules described for the layout of MOS devices apply to resistors as well. For example, resistors that are required to bear a well-defined ratio must consist of identical units placed in parallel or series (with the same orientation).

For large values, resistors are usually decomposed into shorter units that are laid out in parallel and connected in series [Fig.4(a)] From the viewpoint of matching and repro-ducibility, this structure is preferable to "serp-entine" Topologies [Fig.4(b)] , where the corners contribute significant resistance.

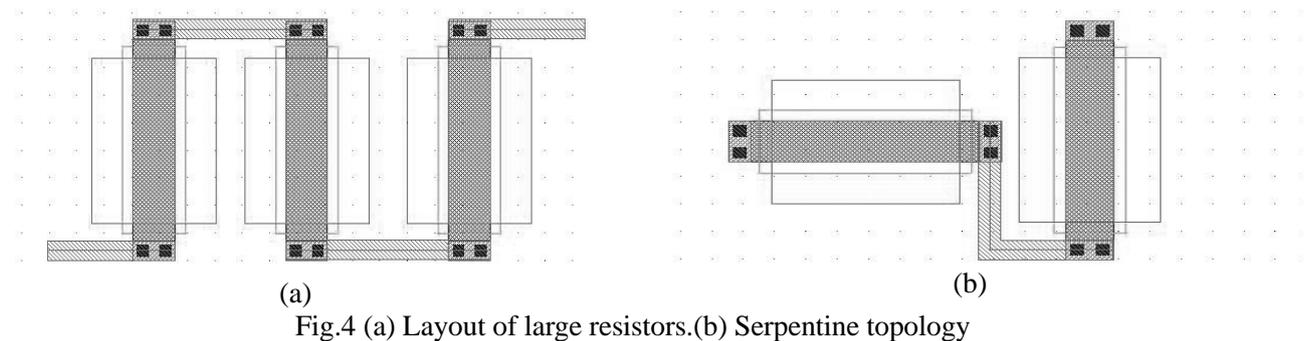


Fig.4 (a) Layout of large resistors.(b) Serpentine topology

## 2.4. Capacitors

Use square geometries for precisely matched capacitors. Peripheral variations are a major source of random mismatch in capacitors. The smaller the periphery-to-area ratio is, the higher the obtainable degree of matching can be got. The square has the lowest periphery-to-area ratio of any rectangular geometry and therefore yields the best matching. Rectangular capacitors with moderate aspect ratios (2:1 or 3:1) can be used to construct moderately matched capacitors, but precisely matched capacitors should always be square(as Fig.5 shows).Oddly shaped geometries should be avoided because it is difficult to predict the magnitude of their peripheral variations.[3]

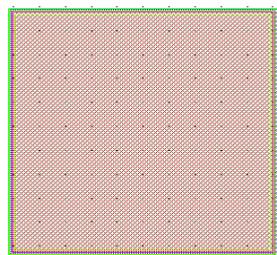


Fig.5 Layout of capacitor

## 3. The layout design of the LDO regulator

### 3.1. Design of Low Dropout linear regulator

As is shown in Fig.6 (a) is the basic structure of LDO regulator. The feedback system formed by RF1 and RF2 of which function is sampling the LDO regulator's output voltage and then put the feedback voltage to the input of error amplifier to compare with the reference voltage. Bandgap voltage reference provides the reference voltage ( $V_{ref}$ ) to the error amplifier, and its accuracy directly affects the precision of LDO regulators output results. The function of error amplifier is to compare the feedback voltage  $V_{fb}$  with the reference voltage  $V_{ref}$ . The output voltage generated by error amplifier adjust the Power Transistor's gate voltage and then change the current flowing through power transistor for the purpose of stabilizing output voltage[4] [5].

The simulation result of proposed LDO as shown in Fig.6 (b) . The simulation tools is Cadence Spectre and the input voltage to the LDO is 4.0V suddenly becomes 5.0V at 0.1ms and lasts 1ms, then becomes 4.0V at 1.1ms . The output voltage of the LDO is almost stable only has some small fluctuations.

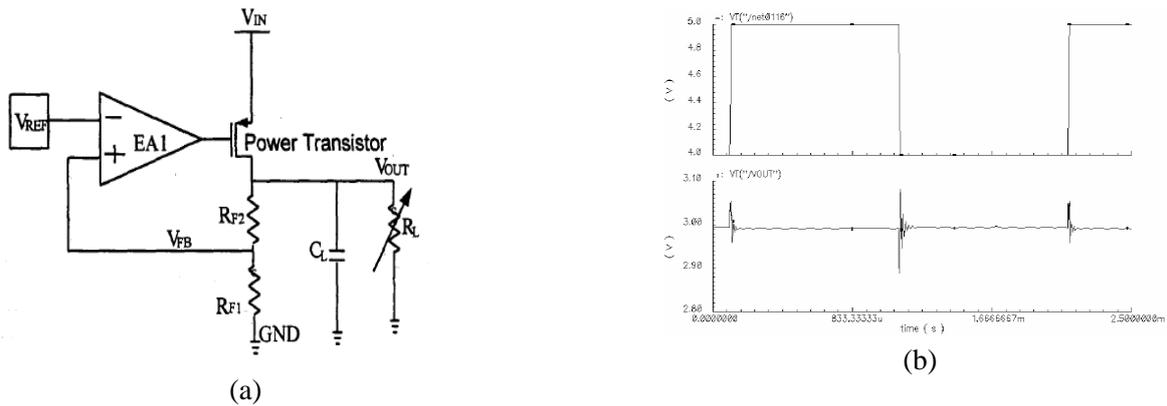


Fig.6 (a) Basic structure of LDO regulator (b) Transient response of proposed LDO

### 3.2. Optimized Layout Design

Error amplifier of proposed LDO formed by differential pairs as shown in Fig.7 (a).M0, M1 MOSFET of differential pairs using multi-finger structure. Due to the voltage of VF and VREF processed by differential pairs, thus, we should use symmetry structure. The layout of the differential pair is shown in Fig.7 (b).The optimized layout of differential pairs ensured the accuracy of input and feedback signal transmission and processing .The resistor layout of LDO assembled by using three series-wound equal-valued resistors. And shorter units are laid out in parallel (shown at Fig.7 (c) below).The shape layout of capacitors we use is square geometries. The whole layout design of LDO manually using Cadence's Virtuoso and the chartered 0.35um CMOS process, as is shown in Fig.7 (d).

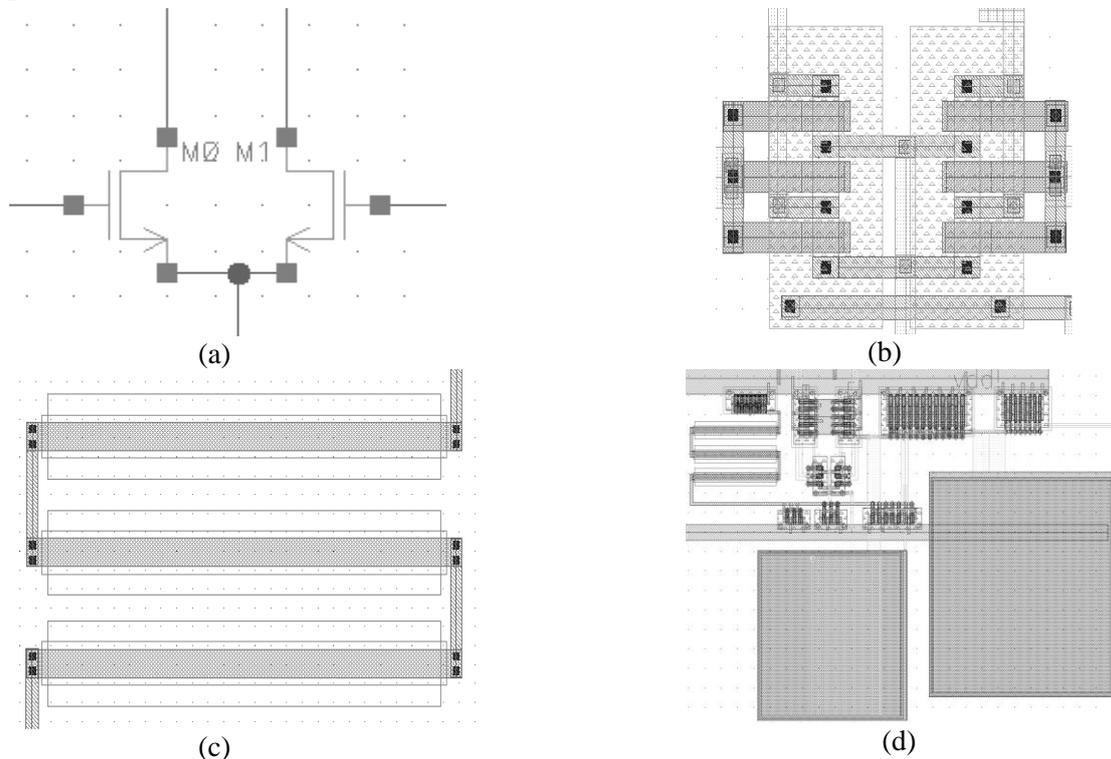


Fig.7 (a) Schematic of differential pairs (b) Layout of differential pairs (c) Layout of resistors (d) Layout of LDO.

### 4. Conclusion

This paper presents some optimized layout design methods and using the EDA tools (Cadence Virtuoso) designed the optimized layout of LDO regulator and the technology is chartered 0.35um CMOS process. This proposed layout of LDO is more precisely matched with the schematic. Through the analysis of these several

optimized methods we can know that reasonable and scientific design approach is necessary and for more complex analog circuits, physical design is also one of the factors affecting their operating performance. However, the realization of a good layout requires more work experience of a physical design engineer.

## **5. Acknowledgement**

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