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A High-Resolution Hybrid DPWM Circuit for Digitally Controlled Buck Converter in 0.13μm CMOS Process

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Abstract. This paper describes a structure of high-resolution hybrid DPWM(Digital Pulses-width Modulator) for digitally controlled Buck converter. In this structure, delay line structure and DLL(Delay-locked Loop) are utilized to realize high resolution of DPWM circuit at high switching frequency(2MHz). The purposes of this circuit are fine time resolution and low power consumption. The proposed digital-analog mixed structure is designed for a Digitally Controlled Buck Converter in 0.13μm CMOS Process.

Keywords: DPWM, DTC, DLL, Delay line

1. Introduction

With the development of strict demands for the performance of DC-DC converters, digitally controlled DC-DC converters become more and more competitive than the analog rivals in recent years. Digital controllers have inherently lower sensitivity to process and parameter variations. High switching speed and low voltage with high power efficiency have been critical requisitions to the converter. Fig.1 shows the classic structure of digitally controlled Buck converter[1]. The digital control system consists of low power ADC(Analog-Digital Converter), high resolution DPWM(Digital Pulse-Width Modulator) and mature compensation algorithm. Among all of them[2], DPWM plays a significant role. A high-resolution DPWM circuit is one of the critical blocks for successful practical realization of digital control for switching power converters.

The high resolution is able to measure the high switching frequency of the controlled circuit. When accepting the measured digital code, DPWM would send out a square wave which has a determined duty ratio to control the Buck Power Stage. To be utilized in the digitally controlled DC-DC converter effectively, there are two main requirements for the DPWM: the first requirement is that the resolution of DPWM should be higher than the resolution of ADC to avoid limit cycling[3]; secondly, it requires the output of DPWM should have a good linearity[2].Here introduce the paper, and put a nomenclature if necessary, in a box with the same font size as the rest of the paper. The paragraphs continue from here and are only separated by headings, subheadings, images and formulae. The section headings are arranged by numbers, bold and 10 pt. Here follows further instructions for authors.

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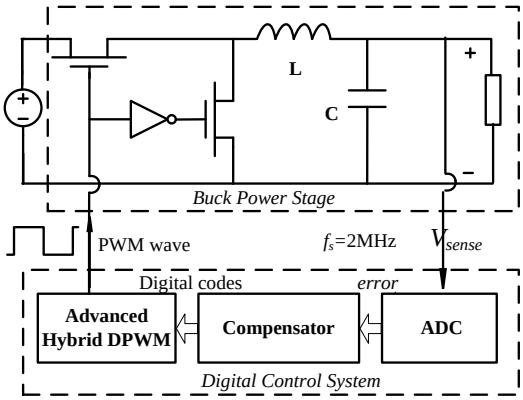

Fig. 1. Block Diagram of the Classic Structure of Digital Controlled Buck Converter

The paper is organized as follows: In Section 2, the classification of DPWM will be introduced. Section 3 will show the configuration of hybrid DPWM which has two elementary parts, coarse DTC and fine DTC. The structure and principle of the proposed DPWM will be showed in Section 4, including a Two-stage delay line structure and an advanced DLL. In addition, the experimental result and simulation is shown in Section 5.

Based on the theory in[4], the proposed hybrid DPWM, which has been improved, is designed for 10-bit resolution, working stably at 2MHz switching frequency. In addition, this circuit is a digital-analog mixed IC.

2. Classification of DPWM

There are three types of DPWM widely used in recent years. They are Dither DPWM, Σ-Δ DPWM and delay-line DPWM.

- Dither DPWM consists of Digital Clock Management (DCMs), a fast counter/comparator block and a dithering approach[5]. This structure utilizes the theorem of frequency-multiple and phase-shift which can improve the resolution of the whole circuit. However, although the particularly complicated proposed circuit is designed, the accuracy of frequency-multiple and phase-shift cannot be measured. Moreover, because of DCM, dither DWPM can only be designed in FPGA rather than in the area of ASIC.
- Σ-Δ theory has been widespread for many years[6]. Utilizing this theory, DPWM can achieve high resolution through two or more stage structure, while more adders and multipliers are needed. At the same time, power consumption will also be exactly high.
- Hybrid delay-line DPWM is the modest module in recent years which consists of two complementary circuits to measure the fine resolution and coarse resolution[4][7][8]. The proposed DPWM is an improved digital-analog mixed one with two delay-lines and DLL.

3. Hybrid DPWM Configuration

DTC stands for Digital-to-Time Converter, which is able to convert digital codes input into timing output. The proposed hybrid DPWM is constructed by two complementary circuits, coarse DTC and fine DTC, shown in Fig.2[4][7]. The coarse DTC translates its output signal - CLKin- to fine DTC as its input signal. The input digital codes are divided into high-bit and low-bit. High-bit codes would be sent into the coarse DTC, while the low-bit codes would be the input signal of fine DTC. Pragmatically, the 10-bit resolution DPWM is divided into a high 4-bit part and a low 6-bit part.

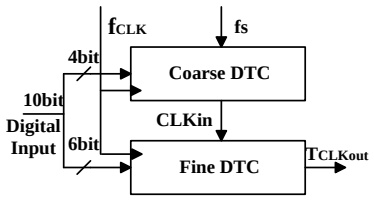

Fig. 2. Block Diagram of the whole Hybrid DPWM

3.1. Coarse DTC

Coarse DTC is often made by a counter and a comparator. The proposed one, which is a digital structure, consists of a 4-bit digital counter and a digital comparator. The digital comparator compares the higher 4-bit of the digital input with the counter output, where the input signal of counter is a 32 MHz clock signal. In Coarse DTC, there is a one-cycle waveform which the period is 31.25ns because the 2MHz switching frequency is the demultiplication of the 32 MHz frequency. The digital counter operates with 32 MHz frequency clock. When the higher 4-bit digital input equals the sum of the counter output and number one, the signal CLKin would be set to high from low so that a square wave which the length is 31.25ns will be generated. In general, the resolution of coarse DTC is called T_{clkin}, where the value of T_{clkin} is 31.25ns(1/32MHz=31.25ns). The Coarse DTC often is a digital circuit.

3.2. Fine DTC

Delay-line structure in DPWM is acted as the fine DTC. Traditional delay-line structure consists of a line of delay cells and a multiplexer[8]. While the resolution of DTC would be 6 bits, it is essential that there exists 63 delay cells(2^6-1=63). As the problem of the fineness of the resolution, and the power and area consumption are extremely high, it is reasonable that the traditional fine DTC should be replaced.

4. Advanced Hybrid DPWM

In order to avoid the shortcomings of traditional structure, the two-stage delay-line structure is proposed. Fig.3 shows the structure of improved circuit. This structure acts as the fine DTC. It can be proved that the number of delay cells would be reduced significantly by the use of proposed fine DTC instead of traditional one.

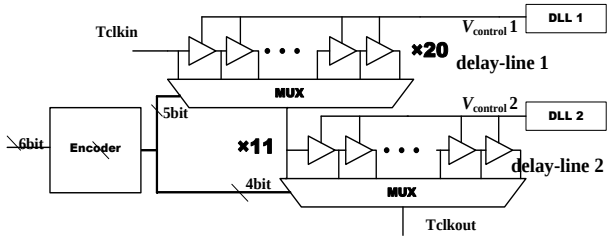

Fig. 3. Structure of the advanced DTC in Hybrid DPWM

4.1. Algorithm and Architecture of Improved Delay-line

The objective of the proposed fine DTC is to achieve fine resolution with small power and hardware. Through a new algorithm performed by the encoder, the low 6-bit input PID codes could be translated into a 9-bit code, sending to two multiplexers to select the correct way which guides the input wave getting through. In this architectural, the encoder can be replaced by a look-up table. The look-up table, which is also the digital module in the whole circuit, should be programmed by the HDL(hardware description language). DLL(Delay-locked Loop) is able to measure the delay time of each buffer in delay lines. Standard 32MHz clock and DLL determine each delay value τ_1 and τ_2 of buffer in delay line 1 and 2. With a simple example Fig.4 will introduce how to select the correct path through the algorithm[4].

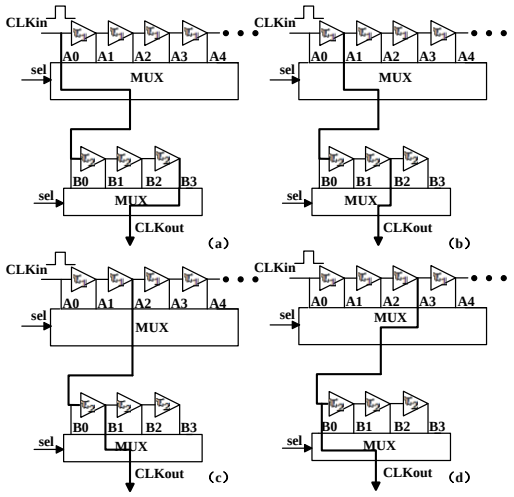

Fig. 4. An Example for the Algorithm in Fine DTC

The resolution of two-stage delay-line is determined by the subtraction of two-stage cell's delay time($\Delta\tau=\tau_1-\tau_2$) instead of the delay time of one cell, where τ_1 and τ_2 mean the delay time of delay cells in delay-line 1 and delay-line 2. This part offers a huge challenge in the whole circuit. How to determine the number of delay cells relates to the algorithm. Assume the number of delay-line 2 is N, where N=3 in Fig.4, the number of cells in line 2 depends on the algorithm. Relationship between τ_1 and τ_2 would be:

$$\tau_2=\tau_1 N/(N+1) \tag{1}$$

In Fig.4, there exists 20 potential paths could be chosen. Determine the first way: the input wave is translated into multiplexer-1 from the port A_0, and sent into multiplexer-2 through the port B_3 in stage-2. As soon as the input code pluses one, the input port would be moved to A_1, while the port in stage-2 is translated to B_2. Every time the input code pluses one, the input port would move a step to the next one, while the port in stage-2 would step into the smaller number on the contrary until the path that these two ports are A_3 and B_0 in turn. This is one period for the algorithm. At the beginning of the next period, chosen ports are A_1 and B_3. With this measure, there are five periods in this example. The last path chooses the input port A_7 and port B_0. The difference of transmission time of each path determined by the border code is $\Delta\tau$, which is the minimal time in the architecture.

The algorithm shown above is also suitable for the complicity construction. Through the same regulation, the number of each delay-line could be determined in the proposed structure. It is reasonable that the number of delay cells in the delay-line 1 is twenty as soon as the number in delay-line 2 is eleven. In order to achieve the proposed highest resolution, the wave sent from the coarse DTC would be divided into 64 parts equally. According to the equation 1, the minimal numbers of N would be 8. In this situation, there are 72 potential paths. However, the fineness of the error is low. Assume $\tau_1= T_{clkin}/11$, $\tau_2= T_{clkin}/12$, so there exists 132 paths translating the square wave. Using an encoder to choose 64 paths from the whole 132 paths is a simple way to raise the accuracy so that the fineness of error has been raised 10 times. Thus, the best choice for N is 11. Through the algorithm, the number of delay cells of two stages can be determined. There are 20 cells in delay-line 1, at this time the number of delay cells in delay-line 2 is 11. What's more, the area and power assumption of it are not much higher than these in the situation that measures 8 cells to the delay-line 2. The delay time of one buffer in each delay line could be determined by DLL(Delay-locked Loop).

4.2. Advanced Delay-locked Loop

DLL is able to measure the delay time of each buffer in delay lines. A typical DLL shown in Fig.5 consists of a Phase Detector, a Charge Pump and a Voltage-controlled Delay Line. The basic function of DLL is calibration, to overlap the feedback signal and the standard signal accurately. The classical structure of DLL is a closed loop, which has an output connecting to one input port-FB.

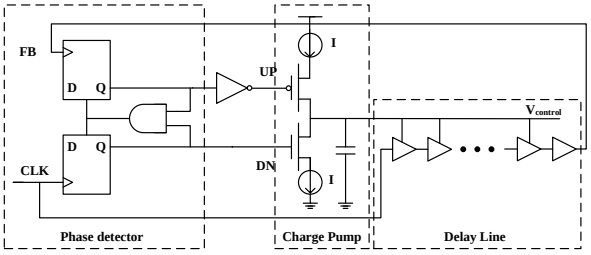

Fig. 5. The Architecture of Typical DLL

While the circle is stable, the feedback signal and the standard signal are overlapped, the DLL will generate a stable controlling voltage to control delay cells outside.

The Phase Detector discriminates the subtraction of phases from two signals, one is from the port FB, the other one is the standard 32MHz frequency clock signal. In addition, the frequency of these two signals should be equal in the DLL. After the phase detection, the detector generates two signals, UP and DN, to the Charge Pump. When the difference of phase of CLK and FB is positive, in the ideal case, the wave sent from port UP would be positive while the wave from port DN is a low logic-level; one the contrary, port UP will give out nothing but a zero level while the output wave from the port DN would be positive. Through the influence of signal UP and DN on the PMOS and NMOS in turn, the capacity is charged or discharged by the current source or current sink. At the same time, the delay time in delay cells is controlled by the controlling voltage. Through this regulation, the circle would be stable finally. At this time, there is a stable controlling voltage having a measured value. It means that the DLL has been locked. Though the typical structure can reach the goal, this circle may be unlocked in practice. The causes of this condition vary from plenty of factors, the main one is that it is totally possible that the controlling voltage would raise to the voltage of source(VDD) in the end.

Because of the potential risk, the structure of DLL can be improved into a structure shown in Fig.6. Based on the typical structure, the Charge Pump is changed: an added MOSFET that the function is reset the controlling voltage. Besides, the function of reset is added to the normal Phase Detector. As soon as the whole circle is beginning, the signal of Reset will make the capacity full at first time. While the signal of Reset is cancelled, the improved DLL, working as the normal process will do following the regulation. Through the improvement in Phase Detector and Charge Pump, the DLL couldn't be unlocked except the damage of the whole circle.

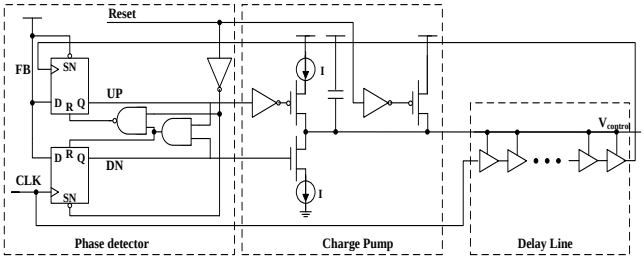

Fig. 6. The Improved Architecture of DLL

5. Experimental Result

The whole structure of the proposed DPWM is shown in Fig.7. A standard 32MHz frequency clock signal is sent into the DPWM. Because of the 4-bit counter, the switching frequency of f_{clk}=32MHz/2^4=2MHz is shown in Fig.8 through the frequency doubling of 32MHz clock signal. Fig.8 depicts the timing sequence of the whole procession in a 2MHz period. This is a synchronous circuit.

Fig.9 shows the simulation of the advanced DLL. Galvanized by the standard 32 MHz frequency signal, the proposed DLL is in the unlocked situation in the first few period. As soon as the signal of Reset appearing, the voltage of controlling signal raises to the value of source voltage(VDD=1.2V). While the

Reset signal cancelled, the whole circle is acting normally. Until the time arriving about 500ns, the controlling voltage seems to be stable. At this time, the action of charging or discharging has already finished, the value of controlling voltage is stable to the value of 508mV. At this time, the proposed DLL has been locked.

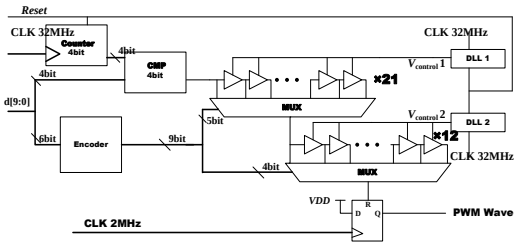

Fig. 7. The whole Structure of Proposed DPWM

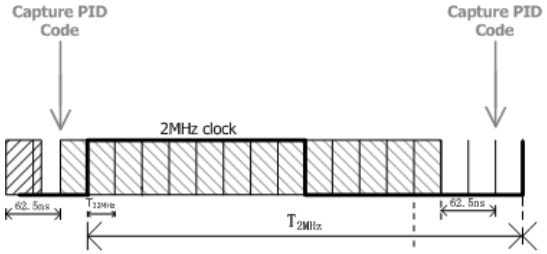

Fig. 8. The timing sequence of the whole procession in a period

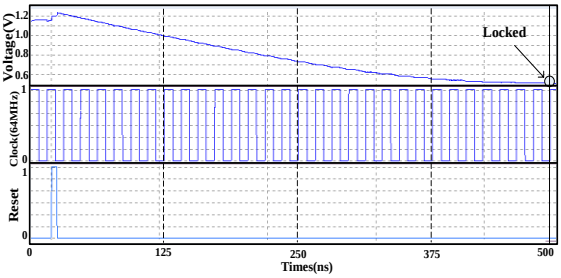

Fig. 9. The Simulation Result of Advanced DLL

The simulation of the whole proposed DPWM is shown in Fig.10.

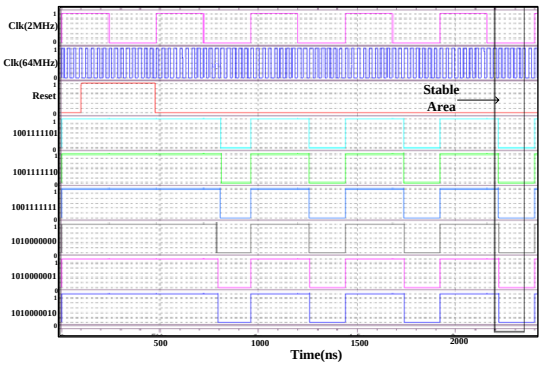

Fig. 10. The Simulation Result-1of the Whole DPWM

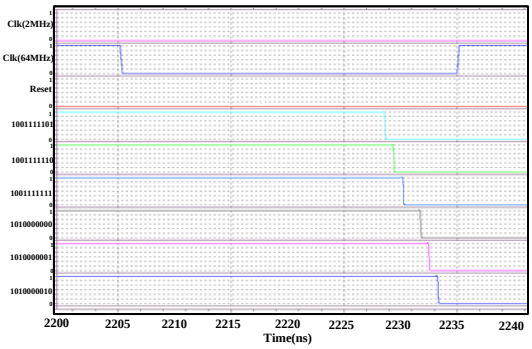

Fig. 11. The Simulation Result-2 of the Whole DPWM

In order to check whether the function of the whole circle is suitable for the design, the output of DPWM should be linear and single. Utilizing the input codes varied from 1001111101 to 1010000010, the proposed DPWM would generate six different output signals shown in Fig.10. To enlarge the rectangle domain in Fig.10, Fig.11 shows that the duty ratio of output signal of DPWM increases linearly and monotonously with the increase of input digital codes. The duty ratio of output square wave varies from 0 to 92.87%.

In conclusion, it could be concluded that this circuit can realize the function of a 10-bit DPWM which the minimal resolution is 488ps.

Fig.12 is the die micrograph of the Digitally Controlled Buck Converter which is implemented in 0.13μm digital-analog mixed signal standard CMOS process. There are more than 30000 transistors in the whole chip which integrated a power MOSFET. The square measure of the chip is about 1.5mm^2.

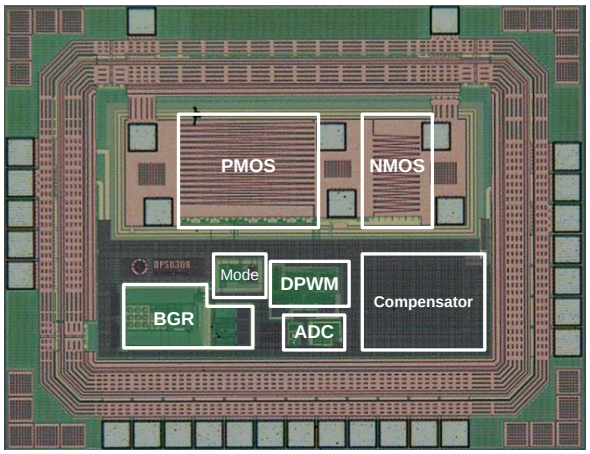

Fig. 12. Die Micrograph of Digitally Controlled Buck Converter

6. Conclusion

This paper describes a High-Resolution DPWM Circuit for Digitally Controlled Buck Converter in the digital-analog mixed way. Though the resolution of DPWM determines the performance of the whole buck converter, the improvement of the resolution should also consider the power and area consumption. The Coarse DTC and the look-up table design is based in hardware description language (HDL), and takes advantage of modern EDA tools for digital ASIC design. At the same time, the stability and resolution of the whole DPWM is improved as soon as the assumption decreases compared with conditional one delay-line structure. In addition, the improvement of DLL is the key factor to the realization of the proposed DPWM.

7. Acknowledgements

Thanks for the assistance of Hou Sijian in this project gratefully.

8. References

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