

An Improved Micro Hard Disk Read-Write Channel Servo Signal Simulate System Design on FPGA

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Abstract. It's important to simulate micro hard disk read-write channel servo signal for design and test. This paper researches a programmable signal generator by an improved high integrated direct digital frequency synthesis (DDFS) technology to simulate servo signal for read-write channel of micro hard disk. This device use very large-scale integrated circuit FPGA (field-programmable logic) to integrate high speed PDSP (programmable digital signal processor) design and DDFS design. Test results indicate that this device has higher precision and sequence of signal, and the circuit need not connect filter and can output 2-256 order harmonious. The circuit design is simply, reliable, and programmable, compared with general design by separate parts design.

Keywords: servo signal, PDSP, FPGA, direct digital frequency synthesis (DDFS)

1. Preface

It plays an important role in the studying of read-write channel of micro hard disk by simulating all kinds of servo signal through high-quality signal generator. The direct digital frequency synthesis (DDFS) is the key technology of designing the signal generator for the time being, which influence the indexes of signal precision, resolution, stability and wave distortion.

Currently, we generally use the traditional design solution of discrete device and integrated circuit, but with complicated circuit design, big circuit consumption and noise interference, less points of each wave circle, and also need to connect to filter circuit, so it has the disadvantage of low signal precision and unable to repair on site.

This paper introduces a kind of 0.0001Hz-25MHz servo signal generated by high-integrated direct digital frequency synthesis, which adopts the total design of high precision

24bit D/A converter and signal generator, please refer to Figure 1 for the general design principle. The extra-large scale FPGA integrates the high-speed PDSP, 4K*24bit RAM and digital frequency synthesis calculation. It utilizes the signal discrete points calculated by PDSP, which contains the amplitude value and phase information, and then store the points in RAM. There are 1024 points in each cycle for this solution. Signal wave table is stored in RAM, which size

is 4K, the pulse signal generates the cycling address through the counter, and then fetch the 24bit binary code from RAM, and then send into D/A converter and output the smooth and continuous signal. Amplitude precision of signal is 0.02%, stability is 0.002%/min, phase precision is 0.02°, and frequency precision is 0.0001Hz, can overlay 2 to 256 harmonic.

2. Direct Digital Frequency Synthesis

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Direct Digital Frequency Synthesis, short for DDFS, is a kind of new frequency synthesis technology developed in recent years, which imports the advanced digit treatment theory into the field of signal synthesis, and signifies the synthesis technology enters the third generation. Its feature is to synthesize frequency by PC, and change the digit signal into analogue signal by D/A converter, and then carry out the frequency synthesis in the time domain. DDFS has the main advantage of: short time of frequency convert (to ns grade), phase and amplitude can be program controlled, same stability of output frequency and clock. Figure 2 is the basic schematic diagram of DDFS system.

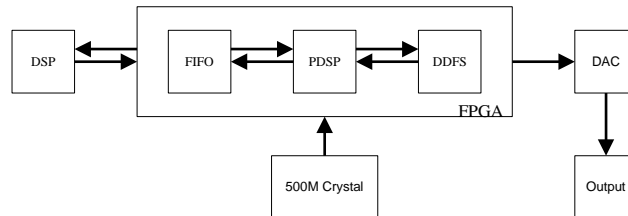


Fig. 1. integrated design schematic diagram

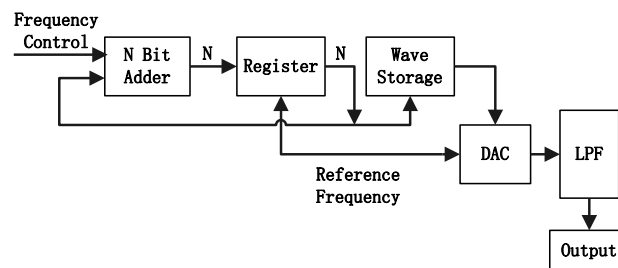


Fig. 2. basic schematic diagram of DDFS system

2.1. Traditional Design of Direct Digital Frequency Synthesis

Frequency divider works in the way of 74LS191 4-digit addition-subtraction counter and cascade connection with four chips. Addressing addition counter circuit is realized by using 74LS283 all adder cascade mode. If Module 1024 adder circuit needs to use three chips 74LS283, signal wave pre-calculate it and put into the storage. The disadvantage of this solution is: complicated circuit design, unable to change the design on site, high circuit consumption, bad precision and signal quality.

2.2. Improved Design of DDFS based on FPGA high integration

Frequency divider, adder and lookup table is realized by FPGA, and the information of signal wave form, such as frequency, phase and amplitude, should be real time converted by DSP, and send into FPGA. Because of the programmability, flexibility and fast-speed of FPGA, it has been developed rapidly and widely applied in the design of digit circuit and digit signal process [2] [3]. The PDSP based on FPGA integration design and the Direct Digital Frequency Synthesis is becoming increasingly salient in the field of digit signal process, because of it high-speed process, flexible modification, especially the capability at digit signal process [4][5]. This paper bases on the technology of Direct Digital Frequency Synthesis [1], and it designs the special PDSP and Direct Digital Frequency Synthesizer according to the advantages of FPGA. Compared with realization mode in the past, it can reduce the quantity of components and disturbance on circuit, and increase the signal stability and also can be modified on line.

3. Realization of PDSP and Direct Digital Frequency Synthesizer in FPGA

Compared with external connection to DSP, it has the advantage of higher flexibility, more convenient modification, and lower cost to realize PDSP in FPGA. Here we only use the basic function of DSP. Direct Digital Frequency Synthesis is based on concept of phase, and it is a new frequency synthesis technology to directly synthesize the wave form in need. It far surpasses the traditional frequency synthesis technology in series of indexes, such as relative bandwidth, frequency conversion time, continuity of phase, quadrature output, high resolution and integration, etc.

3.1. Realization Course of DDFS

The phase adder is cascade connected by N-digit full adder and N-digit accumulation register, which is capable for accumulation calculation of binary code of frequency control word. It is a kind of typical feedback circuit, and the high M-digit of accumulation result generated can be the sampling address value of RAM of look-up table, in this way, a periodical signal wave value is stored in the look-up table. Obviously, here the storage RAM can be considered to be a converter from phase to amplitude value. So, it can drive the D/A converter by RAM output value, and then convert into the simulation signal wave form in need through the filter. At the same time, the N-digit accumulation output can also be considered to be the next round date of full adder to add with the frequency data, until the 16 bit phase adder is full with overflow, and finally a circle is finished, this is the frequency circle of DDFS signal.

3.2. Realization of DDFS in FPGA

The design of FPGA contains three parts:

- Design of look-up table calculation: To calculate 1024-point dispersed wave form according to the frequency, phase, and amplitude of signal, and then store in RAM, so it is needed to design a 4K*24bit RAM and 24bit*24bit multiplier unit.
- Design of DDFS calculation: Use 16 bit frequency divider as the clock of 32 bit adder to input, 300MHz clock is adopted for frequency divider to input, so the high bit of adding result of adder can be the addressing of RAM.
- Design of read-write controller of RAM and D/A converter: Design of data bus, address bus, control bus of read-write operation for RAM and D/A converter.

3.3. Realization of PDSP in FPGA

The PDSP function is realized by designing a 24bit*24bit multiplier and a 32bit summator.

In this design, we adopt FPGA chip Cyclone IV EP4CE6E22I8N provided by ALTERA Company to realize DDFS and PDSP. EP4CE6E22I8N is the latest product of ALTERA for DSP and multi storage application, which supports high speed core and I/O, with optimized internal storage and flexible I/O. The number of Adaptive Logic Module (ALM) of EP4CE6E22I8N is 19000, the number of logical equivalence unit (LE) is 47500 and 1836(Bits) embedded array block, which can provide max. 144KB ROM/RAM bit, so it can meet the design requirement of DDFS and PDSP.

The circuit design of FPGA is realized by using VHDL hardware description language, because VHDL hardware description language can be planted into different FPGA chips conveniently. In this system, the external connected crystal of FPGA has the highest frequency of 500MHz, can be said as a high speed system. So when laying the PCB, should pay attention to isolation in case of the noisy disturbance, and also should avoid the burs when inducting the clock. In addition, also need to take some measures to increase the running speed, such as the flow line technology and design the high speed circuit by using the carry chain of FPGA device. Figure 3 shows the simulation of DDFS realization course, among of them, signal ADDER is the coursing of address adding, 80M_CLK is the clock after frequency dividing, OUT is the pulse output. Figure 4 is the design simulation of look-up table calculation, RAMADDRESS is the address generator of RAM, and INTEGER_COUNTER is the multiplier.

Design of main module design of DDFS: DDFS can refer to above principles, to describe by VHDL, and below is part of the original program of calculation.

```

BEGIN
PROCESS(CLK)
BEGIN
COUNTER[31..0]=COUNTER[31..0]-1;
CLK=COUNTER[31];
IF(CLK' event AND CLK='1') THEN
\\ clock rising edge trigger
FREQ<=FREQINPUT;
AC0<=AC0+FREQ; \\adding
END IF;
END PROCESS;
RAMADDR<=AC(ADDER WIDTH-1 DOWN TO ADDER WIDTH-16); □ \\ high 16-digit of adding
result is the address bit of look-up table

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RAM: LPM_RAM\ calling of RAM look-up table

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Design of DDFS control module: The system control of DDFS is designed based on the necessary functions, such as phase modulation and amplitude modulation, this is a kind of utilization of flexibility of FPGA. The schematic diagram is referred to Figure 5.

Design of PDSP control module: PDSP is designed for look-up table, also a kind of utilization of flexibility of FPGA. The schematic diagram is referred to Figure 6.

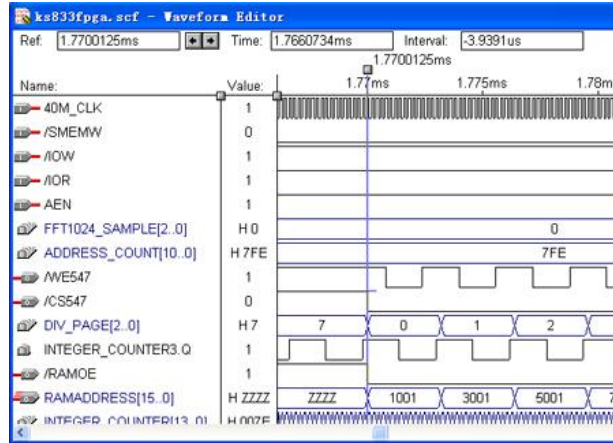


Fig. 3. DDFS simulation

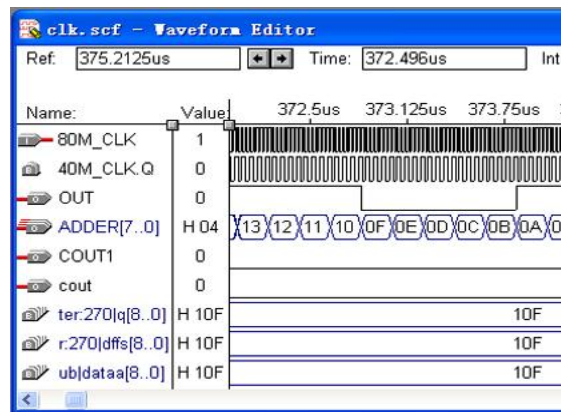


Fig. 4. PDSP simulation

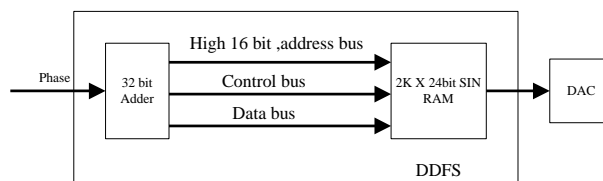


Fig. 5. DDFS design schematic diagram

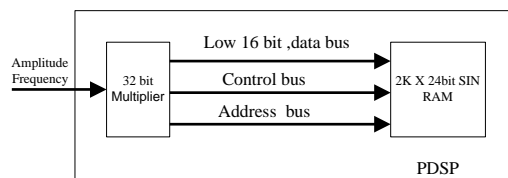


Fig. 6. PDSP design schematic diagram

3.4. Comparison of Test Result

The comparison test result of this design and tradition design is referred to Table 1, 2 and 3, for the comparison of precision of amplitude, phase and frequency. It can be indicated that the precision is increased a lot, and the design has meet the expected result.

Table 1. Improved scheme test result compare with traditional scheme on amplitude

Amplitude (V)	Improved scheme (V)	Error (%)	traditional scheme (V)	Error (%)
0.1	0.10002	0.02	0.10050	0.50
0.5	0.50008	0.01	0.50200	0.40
1	1.00010	0.01	1.00350	0.35
2	2.00025	0.01	2.00640	0.32
3	3.00036	0.01	3.00910	0.33
5	5.00700	0.01	5.01503	0.30

Table 2. Improved scheme test result compare with traditional scheme on phase

Phase (°)	Improved scheme (°)	Error (°)	traditional scheme (°)	Error (°)
30	30.015	0.015	30.031	0.031
90	89.983	-0.017	90.027	0.027
120	120.020	0.020	119.034	0.034
240	240.011	0.011	240.022	0.022
270	270.013	0.013	270.036	0.036

Table 3. Improved scheme test result compare with traditional scheme on frequency

Frequency (Hz)	Improved scheme (Hz)	Error (Hz)	traditional scheme(Hz)	Error (Hz)
1	1.00008	0.00008	0.89154	0.1085
10	10.00001	0.00001	9.76552	0.2354
50	50.00008	0.00008	50.39732	0.6027
100	100.00009	0.00009	100.25752	0.7435
400	400.00005	0.00005	400.46903	0.4310
700	700.00005	0.00005	700.67723	0.3228

4. Conclusion

This paper is an simulate micro hard disk read-write channel servo signal system design on FPGA, and the test result proves the quality of output signal is highly increased compared with the traditional designs, and the effectiveness of this solution is gradually recognized.

5. Acknowledgements

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