

An Overview of Design Techniques for On-Chip Eye-Monitors of Gbps Data Links

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Abstract: This paper presents an overview of design techniques for on-chip eye-opening monitors for Gbps data links. The classification of eye-opening monitors is provided. The design of 1-dimensional eye-opening monitors, 2-dimensional eye-opening monitors, data-edge based eye-opening monitors, and multisampling eye-opening monitors is investigated and their pros and cons are studied. A detailed comparison of the performance of recently reported eye-opening monitors is provided.

Keywords: Serial Links, Eye-Opening Monitors, Clock and Data Recovery.

1. Introduction

Serial links achieve a high data rate by extracting timing information directly from received data, thereby eliminating the need for a dedicated channel for clock transmission and the difficulties associated with clock skew. The data rate of serial links is limited by inter-symbol interference (ISI) arising from the resistive and dielectric loss of channels, cross-talk with neighboring devices, and reflection caused by impedance mismatch at high frequencies. While cross-talk can be minimized using fully differential signaling, impedance mismatch can be mitigated using digital trimming, the effect of channel loss is minimized by employing pre-emphasis at transmitters that purposely lowers the low-frequency components of the transmitted data, and decision-feedback equalization (DFE) at receivers. The effectiveness of pre-emphasis at transmitters is undermined by the fact that the characteristics of the channel over which data are transmitted are not known a priori to data transmission. Decision-feedback equalization has been demonstrated to be the most robust and effective means to combat ISI. A decision-feedback equalizer is essentially a digital filter with the number of the taps determined by the characteristics of the channel. The effectiveness of DFE, however, is greatly affected by the number of the taps, the space of the taps, and the value of the taps of the DFE [1]. Since the impact of ISI is directly reflected by the eye-opening of the received data, DFE is optimized once the eye opening of the received data is maximized.

Traditionally the eye diagram of the received data is obtained using high-speed pattern generators and oscilloscopes, which are prohibitively costly. Expensive high-speed pattern generators have widely been replaced with on-chip pseudorandom generators that generate a sequence of pseudo-random data bits at transmitters. A low-cost on-chip eye-opening monitor that is capable of providing the real-time mapping of the received data to an eye diagram is highly desirable. There has been an increasing effort in design of low-cost on-chip eye-opening monitors for Gbps data links recently. Various design techniques and systems configurations have emerged. An in-depth assessment of the pros and cons of these techniques, however, is not available. This paper is an attempt to provide a comprehensive examination of the state-of-the-art of on-chip eye-opening monitors of Gbps data links.

2. Classification Of On-Chip Eye-Opening Monitors

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On-chip eye-opening monitors can be loosely classified into (i) one-dimensional eye-opening monitors, (ii) two-dimensional eye-opening monitors, (iii) Data edge-based eye-opening monitors, and (iv) multi-sampling eye-opening monitors. An one-dimensional eye-opening monitor quantifies the opening of data eyes by either the vertical or horizontal dimensions of the eyes [2], [3], [4]. One-dimensional eye-opening monitors are the simplest in term of hardware and consume the lowest power. Since only either the vertical or horizontal openings of the eye are used, it yields a poor picture of the quality of the eye. A two-dimensional monitor quantifies the eye-opening by measuring the dimension of the eye in both the vertical and horizontal directions [5], [6], [1]. They are the most widely used eye-opening monitors and require moderate hardware and power. Data edge-based eye-opening monitors quantify the eye-opening by examining the edges of data eyes (threshold-crossing) using multiple samples. They are often power consuming. Multi-sampling eye-opening monitors scan data eyes both vertically and horizontally with a large number of samples per bit time [7], [8], [9]. They are most comprehensive but at the cost of hardware, power, and speed.

3. One-Dimensional Eye-Opening Monitors

One-dimensional eye monitors use only either the vertical or horizontal dimensions of the eye to quantify the quality of the eye. In [3], Bien *et al.* proposed a transition detector-based eye monitor to quantify the dispersion of the received data. Since the dispersion of data over a wire channel is mainly due to the loss of high-frequency components of the transmitted broad-band data, the higher the loss of the high-frequency components, the smaller the eye-opening. Thus the quality of data eyes can be quantified by measuring the amount of high-frequency components of the received data. This is achieved by employing an edge detector that detects the transition of the received data and integrating the output of the edge detector over two adjacent transitions. The amount of transition detected is used a figure-of-merit quantifying eye opening. The same approach was used by Kim *et al.* in [4] for 1.25 Gbps passive optical network upstream links. One-dimensional eye-opening monitors are simple in configuration and low in power consumption. They have been widely used for adaptive DFE due to their simplicity.

4. Two-Dimensional Eye-Opening Monitors

The eye-opening monitor proposed by Ellermeyer *et al.* is shown in Fig.1. The minimum eye opening is defined horizontally by two sampling points t_1 and t_2 and vertically by two threshold voltages V_H and V_L . If $v(t_1) > V_L$ or $v(t_1) < V_H$ or $v(t_2) > V_L$ or $v(t_2) < V_H$, a violation of the minimum eye-opening is detected. Two levels of the severity of violation are defined. As shown in the figure, cases A and B are light violations as in both cases only one violation at either t_1 or t_2 exists. Case C is a severe violation as it has violations at both t_1 and t_2 . Depending upon the severity of violation, different adjustments to the parameters of the equalizer could be used to maximize the eye opening the transition of the received data and integrating the output.

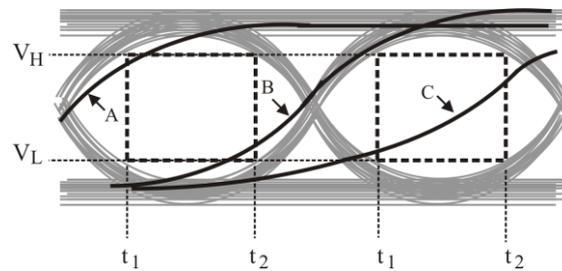


Figure1: 1-dimensional eye-opening monitor proposed by Ellermeyer *et al.*

Fig.2 shows the configuration of Ellermeyer eye-opening monitors. Comparators CMP1 and CMP2 compare the incoming data with V_H and V_L . The outputs of the comparators are latched at the rising edge of Clock-1 and Clock-2 by flip-flops. Clock-1 and Clock-2 are generated from a delay-locked loop and phase shifters. Comparator CMP3 is used to sample the data at the center of the eye to perform data recovery. Three control signals UP (no violation), DOWN (light violation), and BAD (severe violation) are generated, and are fed into a charge pump to generates an analog voltage signal representing the opening of the data eye. This voltage is then used by the DFE to tune its parameters in order to maximize the eye-opening.

In [5] a two-dimensional eye opening monitor, similar to that proposed by Ellermeyer *et al.*, was proposed by Analui *et al.* The vertical opening is determined by two threshold voltages V_H and V_L and the horizontal opening is determined by two sampling clocks ϕ_{early} and ϕ_{late} . The errors at ϕ_{early} and ϕ_{late} are counted separately so as to capture the degree of the asymmetry of the data eyes. Because vertical threshold voltages are placed symmetrically with respect to the common-mode voltage of the input, the vertical asymmetry of data eyes cannot be assessed. Fig.3 shows the configuration of Analui eye-opening monitors. It uses a fully differential comparator with two reference voltages to define the vertical opening, and two sampling clocks $_early$ and $_late$ to define the horizontal opening. After the comparator outputs are latched, they are sent to digital logic stages that combine them and output an error signal every time there is a minimum eye-opening violation. Fig.4 shows three different masks that could be used to estimate the effective eye opening. A combination of these masks provides a good representation of the effective eye opening.

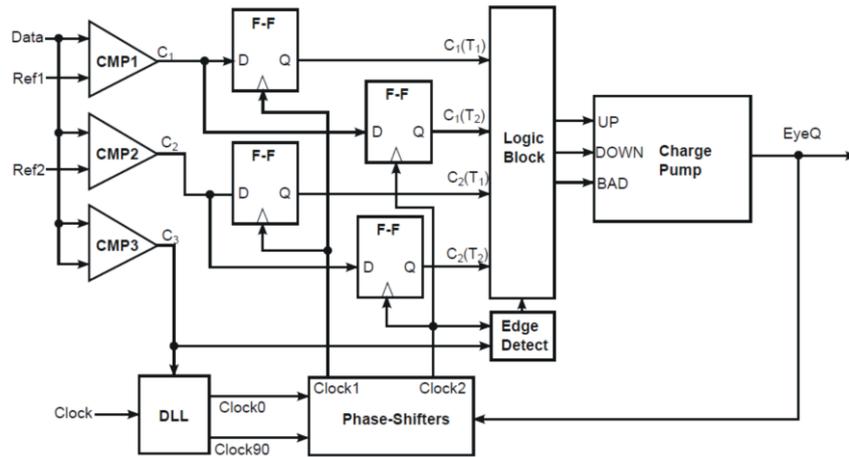


Figure 2: 2-dimensional eye-opening monitor proposed Ellermeyer *et al.*

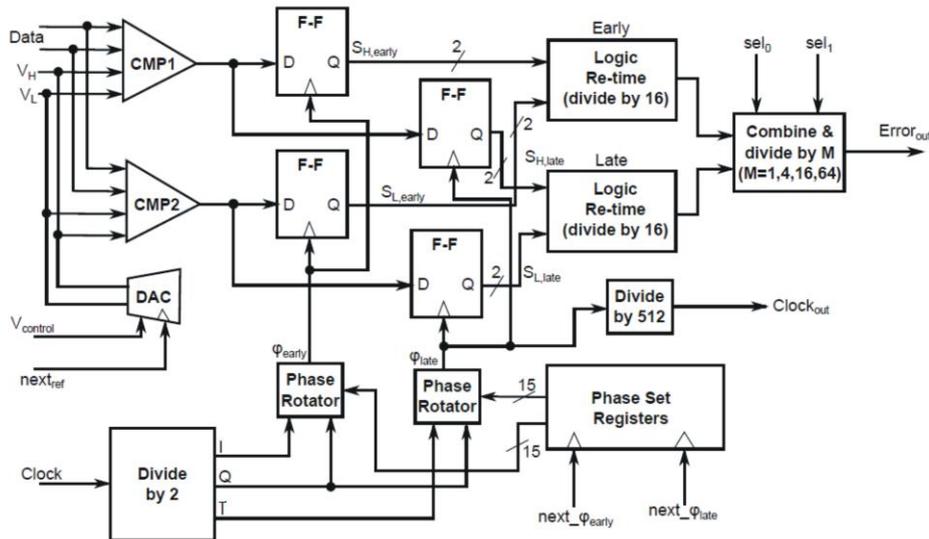


Figure 3: Architecture of 2-Dimensional eye opening monitors proposed in [5],[6].

A similar approach was used in [1] to monitor eye opening. However, this eye monitor only looks at the best fit mask and collects the information from the best fit mask. Another two-dimensional monitor is given in [6] to monitor the eye opening. This monitor not only looks at the eye opening area but also monitors the decision from the CDR. It compares CDR's decision with that of the eye opening monitor and outputs a voltage. This voltage is then compared to three threshold voltages to determine if the CDR and monitor decision are in the same area. The two-dimensional diagram of the eye opening area is obtained by sweeping vertically and horizontally. This monitor allows for timing recovery in CDR applications. An external PC with a control algorithm is required.

5. Data-Edge Based Eye-Opening Monitors

Since eye-opening is determined by both the limited channel bandwidth and the random disturbances, and the impact of the random effects tend to average out over time, the width and shape of the data edge distribution can be used to quantify eye-opening. In [12], a data-edge based eye-opening monitor was proposed. The method is based on a long-term time-domain analysis of the data eye and the edge information of the data eye extracted from data samples are used to quantify the eye-opening. Specifically, the transition edge of data eyes is sampled by a number of samplers, as shown in Fig.5. A set of XOR gates are used to determine the transition edge of the data eyes and counters are used to record the number of transitions at each sampling position. An edge-transition histogram is then generated. Measurement results demonstrate that the larger the eye opening, the narrower the histogram. The histogram thus provides an effective mean to quantify the eye-opening without actually measuring the physical opening of the data eye. Since the quality of the histogram depends upon the number of samplers used, this method tends to be power hungry. Also, it becomes difficult to employ multiple samplers when data rate is high.

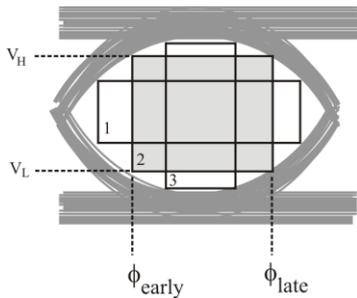


Figure 4. Variable minimum eye-opening mask for eye-opening measurement [5].

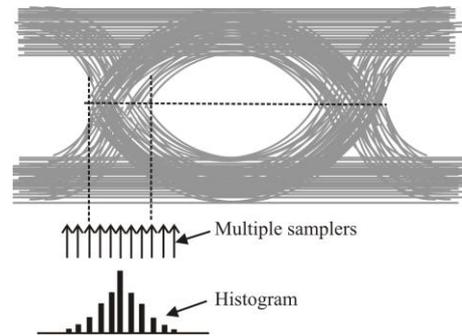


Figure 5. Data edge-based eye-opening monitor by Gerfers *et al* [12].

6. Multi-Sampling Eye-Opening Monitors

A brute-force approach to monitor eye-opening is to sample the data eye multiple times from the left edge of the eye to the right edge of the eye so as to capture the entire eye diagram. For example, the eye-opening monitor proposed by Noguchi *et al.* scans data eyes in 128 steps per bit time [6]. The position with the maximum eye-opening margin in both the vertical and horizontal directions is considered the optimal position for data recovery operation. Since multiple sampling clocks are needed, a precision phase shifter is needed and phase interpolation is used to blend in-phase and quadrature-phase in order to generate the required fine phases. This method is power-demanding due to a large number of sampling operations. A similar approach was adopted by Altera Corp. in its latest EyeQ (Eye-quality-monitor) [9]. Multiple phase steps are used to sample the received data. At each step the bit error rate (BER) is monitored. This in turn provides the horizontal eye opening and the optimal sampling point. The architecture of this eye-opening monitor is given in Fig.6. It consists of a phase interpolator, samplers, and multiplexers. The phase interpolator is used to generate 32 fine phase steps from the recovered clock so that the eye is scanned from the left to the right in 32 steps. The data samplers capture the data in each of the 32 steps and it is either correct or incorrect based on the comparison with the sampling thresholds. The sampling thresholds are set based on the required BER. The multiplexers are used to select between the data recovered by the CDR and that from the EyeQ. An example operation is given in Fig.9. Each sampling point is evaluated with the sampling threshold to determine if it passes the BER requirement.

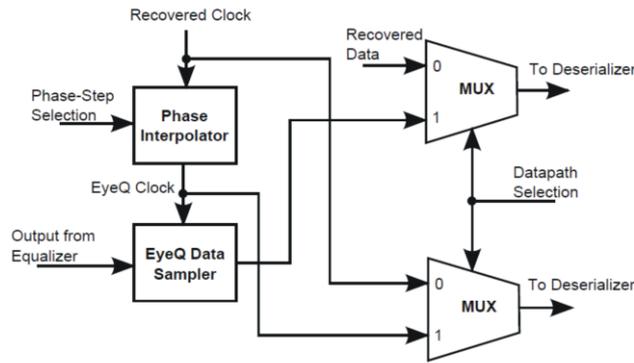


Figure 6: Architecture of multi-sampling eye-opening monitors by Altera Corp.[9].

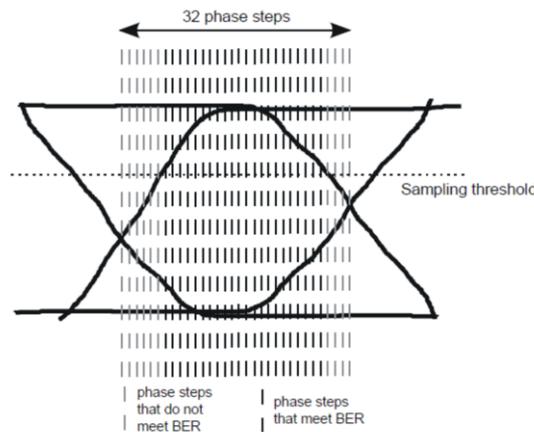


Figure 7: Operation of Altera multi-sampling eye-opening monitor.

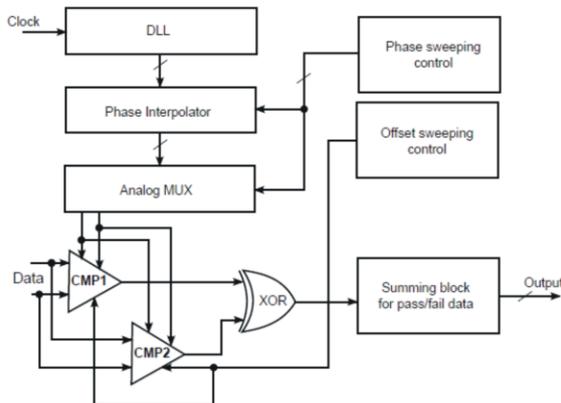


Figure 8: Architecture of multi-sampling eye-opening monitors proposed in [7] and [8].

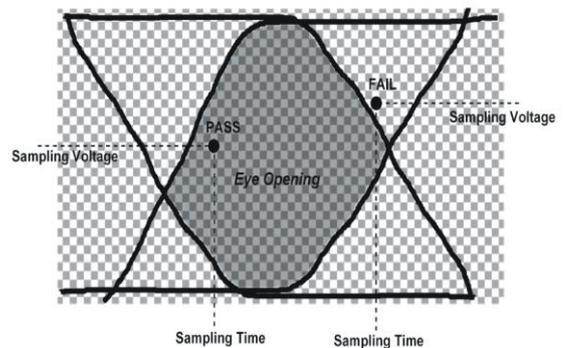


Figure 9: Operation of multi-sampling eye-opening monitors proposed in [7] and [8].

In [7], [8], an on-chip signal integrity analyzer (OSIA) that is based on multi-sampling eye-opening monitor was proposed. OSIA sweeps both horizontally and vertically to capture data eyes. Fig. 8 shows the configuration of OSIA. Essentially, the voltage offset detector block samples the vertical of the eye opening and the multi-phase clock generator samples the horizontal eye opening. The voltage offset detector consists of comparators and a XOR gate. The multi-phase clock generator block consists of a delay locked loop (DLL) and a phase interpolator. This monitor divides the eye opening area into lattices according to the resolution is set by the voltage offset detector and the multi-phase clock generator. The monitor passes or fails data if its lattice is inside or not inside the eye opening area. Since only one lattice can be determined pass/fail at a time. Completing the scan of an eye diagram is time-consuming. This eye-opening monitor, however, provides the most accurate and complete eye diagram. Table I compares the performance of recently published eye-opening monitors. Note that in [4], [3], [6] the performance is based on the entire chip

that includes an equalizer or various other system components whereas those in [2], [5], [1], [7], [8] are only for eye-opening monitors.

Table 1: Comparison of eye-opening monitors.

Reference	Technology	EOM Type	Power Dissipation	Bit Rate
Ellermeyer [2]	SiGe Bipolar	1-D Horizontal	4.95W	10Gb/s
Kim [4]	0.18 μ m CMOS	1-D Vertical	54mW	1.25Gb/s
Bien [3]	0.18 μ m CMOS	1-D Vertical	-	10Gb/s
Analui [5]	0.13 μ m CMOS	2-D	330mW	12.5Gb/s
Noguchi [6]	0.18 BiCMOS	2-D	1.6W	38-42Gb/s
Bhatta [1]	0.18 μ m CMOS	2-D	95mA	5-10Gb/s
Shin [7], [?]	0.18 μ m CMOS	multi-sampling point	-	6.4Gb/s
Gerfers [12]	0.18 μ CMOS	Edge	110 mW	2 Gbps

7. Conclusions

An overview of design techniques for on-chip eye-opening monitors for Gbps data links has been presented. The classification of eye-opening monitors has been provided. We have shown that 1-dimensional eye-opening monitors have the lowest hardware cost but provide a poor quantification of the health of data eyes. 2-dimensional eye-opening monitors are the most popular as they provide both vertical and horizontal measures of data eyes. Data-edge based eye-opening monitors quantify the eye-opening using the statistical information of the edges of eyes. Multi-sampling eye-opening monitors are the most comprehensive at the cost of high hardware and power consumption.

8. References

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