

Design and Implement of CH376 Driver Based on FPGA

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Abstract. This paper introduces a FPGA to read and write files on USB flash disk the specific implementation. The system uses Altera Corporation CycloneIII EP3C5E144C8 chip, CH376 control chip for the read and write, to achieve the above functions. This paper mainly studies how to use the Verilog language to write the serial port on the CH376 driver in the FPGA. The driver through the ModelSim simulation, and has been applied in practical projects.

Keywords: FPGA, CH376, Asynchronism Serial Port

1. Introduction

FPGA(field programmable gate array) is developed based on programmable devices such as PAL, GAL and EPLD, which has high speed, high density, low power consumption characteristics [1]. FPGA chip using ASIC design, both the lack of flexibility in custom circuits can be solved, and related hardware and software environment can grasp the ultimate function of the chip to improve the success rate of a design. Therefore, currently FPGA has been used in the electronic design widely. At the same time, the feature of Verilog HDL is: can formally abstract the structure and behavior of the circuit, support levels and areas of logic design description, you can use the compact structure of high-level language to simplify the description of the circuit with simulation and verification mechanisms, in order to ensure the correctness of the design.

CH376 is used as file manage control chip, used to MCU system read/write file in USB Flash Drive or SD card. CH376 supports USB-Device Mode and USB-HOST Mode. Set the basic firmware of USB communication protocol in the inner. It is also set firmware of special communication protocol to deal with Mass-Storage devices, communication interface firmware of SD card, FAT16, FAT32 and FAT12 file system manage firmware in the inner. It supports common USB storage devices and SD cards .CH376 supports three communication interfaces: 8-bit parallel, SPI interface or asynchronism serial interface. DSP/MCU/MPU etc. controller via the any interface of them to control CH376 chip, storage and get file in USB Flash Drive or SD card, or communication with computer.

2. System introduction

Asynchronous serial signal line includes: serial data input pin RXD and serial data output pin TXD. Through the serial interface, CH376 and MCU, DSP can be a more long-distance connection with the least connection. RXD and TXD of CH376 can be connected to the MCU serial data output pin and serial data input pin respectively.

To the pins and pin described in table 1:

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Table 1. Pin Described

Pin Name	Pin Type	Pin Description
CS	Input	Chip select input, active with low-level.
RST	Output	Power on reset and external reset before enter into SD mode, active with high-level
TX	Input/Output	Interface configure input during internal reset, with pull-up reset. Serial data output of Asynchronism serial. interface after resetting
RX	Input	Serial data input of Asynchronism serial interface, with pull-up resistor

The system serial data format is the standard byte transmission mode, include 1 start bit, 8 data bits, 1 stop bit. The serial communication baud rate is 9600bps.

3. Drive design and application

3.1. Drive design

For FPGA-driven asynchronous serial mode CH376, the command code and parameters need to be transfer by the serial port to control CH376 read and write. File close operations for example: send synchronization code first(0x57 and 0XAB), and then send the command code and its parameters. Thus the data to be sent is (57, AB, 36,01). The commands and parameters are according to datasheet of CH376.

3.2. Design the file reading process

Control CH376 need send synchronous code and command code simply, waiting for CH376 return interrupt status code, FPGA receives interrupt status, analyzes interrupt and deal with interrupt after the CH376 sends interrupt to FPGA.

Take the open file as an example, when the FPGA send the CMD_FILE_OPEN command and the CMD_SET_FILE_NAME command Settings will open files filename, and open files. FPGA will wait for CH376 returns interrupt status code. If open the directory successful, return interrupt status is ERR_OPEN_DIR, the file length is invalid, it is 0FFFFFFFFH. If open the file successful, return interrupt status is USB_INT_SUCCESS, the file length is valid. If doesn't find the appointed file or directory, return interrupt status is ERR_MISS_FILE.

According to the CH376 work mode, design reading files flowcharts as shown in Fig. 1.

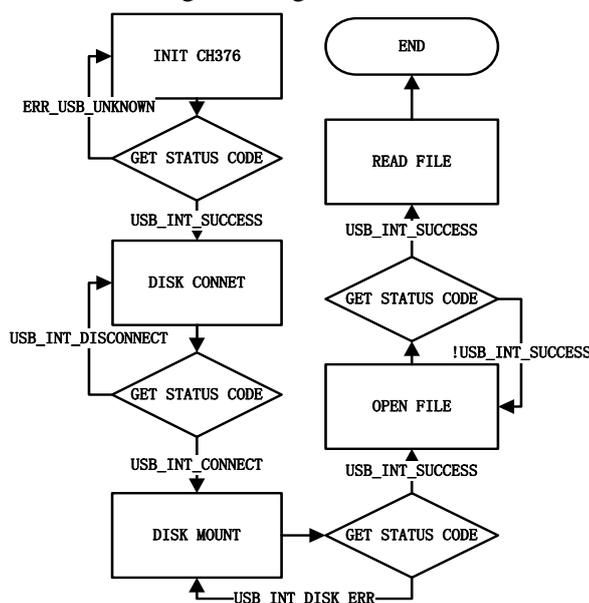


Fig. 1. flow chart for read file

3.3. State machine for read file

When reading files length and the CH376 return right file length , program will entering control documents read state. According to reading files operation requirements, the reading files operating divided into the following several state, Fig.2 shown reach state between the outfit change.

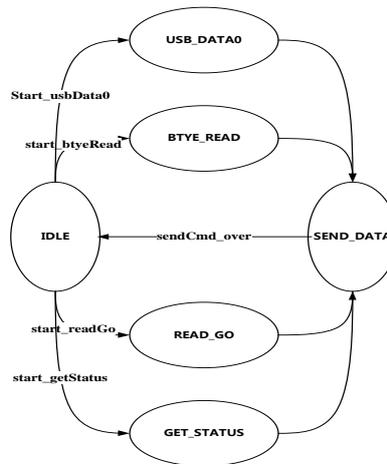


Fig. 2. State machine for read file

To transfer one state to another, Just only need to control the command signal in State Machine. The following list is detail meanings of the start_usbData signal. On the basis of CH376 Datasheet, read file need these command:

- CMD_BYTE_READ is used read data block from current location in bytes, And need to input byte number request to read, the request is based on lower byte in front of two bytes 16-bit data
- .CMD_BYTE_RD_GO is used to continue byte read operation. If read successful, CH376 automatically synchronize move file pointer.
- CMD_RD_USB_DATA0 is used reads data block from current interrupt endpoint buffer of USB or host endpoint. The length of data block is read at first, the data block value is from 0 to 255. If the length is not zero, FPGA reads following data one by one from CH376.

The complete byte read steps follows:

- a) FPGA transfer CMD_BYTE_READ and input byte number which is request, begin read operation go step b;
- b) CH376 calculate the spare length from the current file pointer to the end of location, and send the interrupt notification the FPGA, if the interrupt status is USB_INT_SUCCESS. Go step c , else the interrupt status is USB_INT_DISK_READ, the entire read operation is finished.
- c) FPGA begin read data block through CMD_RD_USB_DATA0 and continue; if it is USB_INT_SUCCESS, turn to step d;
- d) FPAG transfer CMD_BYTE_RD_GO to order CH376 continue read, CH376 automatically turn to step b;

According to the above process, write the program code like below:

```

always@(posedge clk_48Mhz or negedge rst_n)
begin
  if(start_usb_data)
    start_usb_data <= 1'd0;
  else
  begin
    if(read_state_start) //wait Interrupt Status code
    begin
      if(ch376_state_data == 8'h1D)
        // USB_INT_DISK_READ
        start_usb_data <= 1'd1;
        //send USB_DATA0 commend
      end
    else
    begin
      start_usb_data <= 1'd0;
    end
  end
end

```

```

end
end
end

```

4. The simulation result

Along with the logical design and the complexity of increasing, exclusive reliance on software simulation test ways to understand system hardware function have many limitations [5], this system first is used written on Modelsim TestBench waveform simulation, in simulation waveform is correct application Quartus II integrated development environment provided during the Signal- Tap II embedded logic analyzers, will test information with the design documents download from goal chips, to capture target chip internal system Signal node place of information or bus data streams, and does not affect the normal work of the original hardware system. Test information through the device of JTAG port spreads, and return to the computer to carry on the display and analysis.

4.1. ModelSim simulation

Serial command operation steps are as follows:

- FPGA send CH376 the first synchronization code 57H and 0ABH through serial port
- FPGA send command code to CH376;
- If this command have input data, then send CH376 input data in turn, one byte one time;
- If this command have output data, then receive output data from CH376 in turn, e one byte one time;

The ModelSim simulate result is showed by Fig.3 ,Fig.3 is a serial port transmits a command. The system adopted in the clock for 48Mhz, send CMD_BTYE_READ commands and 16bit length of data. In sending data is somewhat different temporal delay in delay according to different clock frequency calculation delay number of cycles, finally achieved delay requirement. As can be seen from the graph, module can correct sends commands.

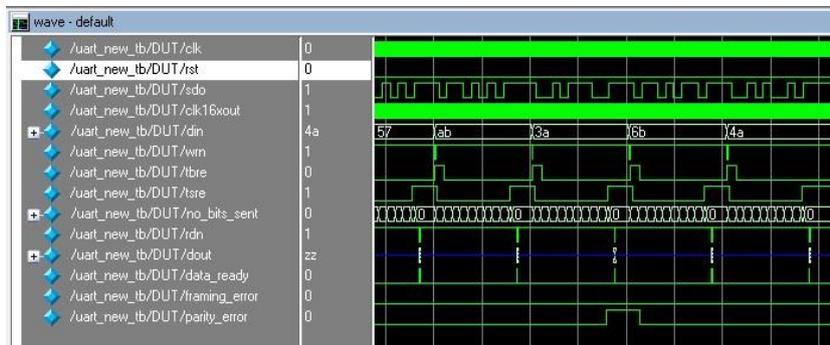


Fig. 3. Send command code Wave simulate by Modlesim

4.2. Signal-TapII analyse

Use JTAG port download procedures and efferent test information, and returns information use Quartus8.0 integrated into the design of software Signal-Tap II embedded in the computer to carry on the logical analyzer display and analysis. The result like Fig.4

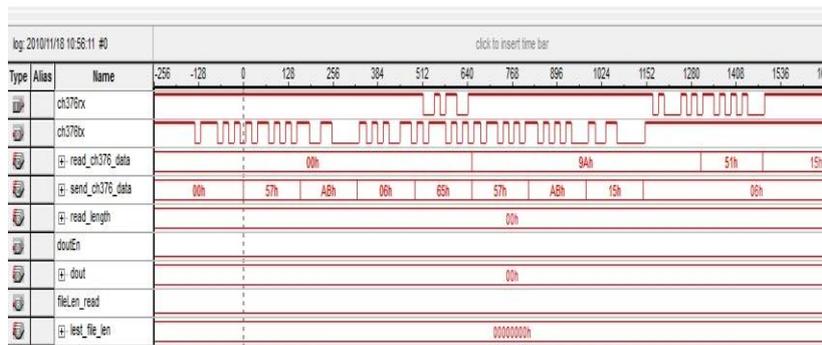


Fig. 4. Send command code Wave analyse by Signal-Tap II

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6. References

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