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EtherCAT Data Acquisition System Based on DMA Mode

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Abstract. Data in peripheral registers can be read without cycle stealing in DMA (Direct Memory Access) mode, which work in parallel with CPU, so it can achieve real-time data processing to great extent. Because of this, when it refers to mass data acquisition, to further improve the real-time performance, a data acquisition system based on EtherCAT in DMA mode is proposed. This paper simply introduces the technical features of EtherCAT technology, analyzes the working principle of the system in DMA mode in detail, and completes the hardware connection and software implementation of the system. The feasibility of the whole system is verified through experiment of multi-channel analog data acquisition.

Keywords: EtherCAT; DMA; PIC microcontroller; data acquisition; real-time

1. Introduction

As network technology advances rapidly, there are extensive applications of Ethernet because of its advantages such as high cost performance and openness, versatility, and good compatibility. It has also been used in industrial control field gradually. Since general Ethernet is not real-time, in order to meet the requirement for industrial control, three methods can be used to convert it to industrial Ethernet: real-time performance is achieved in the application layer with the first method; in the second method priority is set between DLL (data link layer) and application process so that the high real-time demanding task can be processed first; real-time scheduling function is added in data link layer using the third method. The real-time performance of the three strategies rises in sequence. EtherCAT belongs to the third one. EtherCAT Slave Controller (ESC) has Fieldbus Memory Management Unit and SyncManage, which can achieve frame data read and written directly with no necessary to code and encode. The delay of data exchange reaches several nanoseconds, so it has high real-time property and is down to Input (I)/Output (O) level. EtherCAT is a novel high-speed industrial Ethernet and can be applied in real-time data acquisition [1].

In this paper, a data acquisition system based on EtherCAT is proposed. In the slave station, DMA mode is used to complete data acquisition. The microprocessor can read data directly from dual-port RAM of DMA controller without waiting, so it can realize real-time transmission and process of mass data to great extent.

2. Ethercat Technology

2.1. EtherCAT protocol

EtherCAT uses standard IEEE 802.3 Ethernet frames, thus a standard network controller can be used and no special hardware is required on master side. EtherCAT has a reserved Ethernet Type of 0x88A4 that distinguish it from other Ethernet frames [1]. Thus EtherCAT can run in parallel to other Ethernet protocols. EtherCAT data is embedded in the payload of Ethernet Frame. The EtherCAT-specific information starts

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with the EtherCAT-header which is 2 bytes long. The device user data is exchanged by EtherCAT telegrams. Every sub-telegram starts with a 10 bytes telegram header and has at most 1486 bytes data and a relevant working counter. The working counter is automatically incremented by all devices, which process the associated telegram. The master station compares the value of working counter with the expected value. If they are different, it demonstrates the communication failed. It provides an effective diagnostic tool. The main advantage of EtherCAT is based on the possibility to pack the individual data of several devices into one single summation frame. The potential of merging EtherCAT telegrams in one single frame reduces the overhead of EtherCAT.

2.2. EtherCAT slave controller

EtherCAT slave controller achieves data link layer proto-col. Its internal structure diagram is shown as Fig.1. It is responsible for processing EtherCAT data frames, and providing data interface to microprocessor. An EtherCAT slave controller can have an address space of up to 64K Bytes used in exchanging data between master station and slave station [2]. The EtherCAT Processing Unit receives, analyses, processes the EtherCAT data stream. It is logically located between port 0 and port 3. EEPROM is used to store the configuration parameter of ESC and application. Sixty-four bits distributed clock is supported allowing for precisely synchronized generation of output signals and input sampling, as well as time stamp generation events.

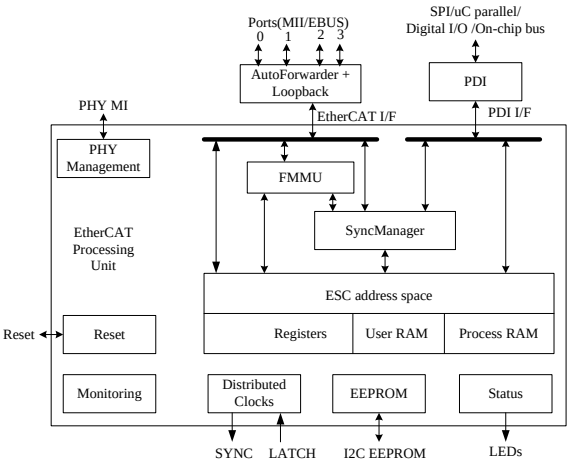

Fig. 1: ESC structure diagram

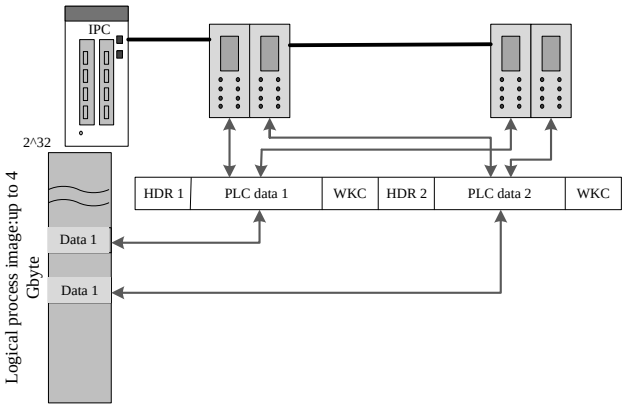

Fig. 2: FMMU operation principle

Fieldbus Memory Management Unit (FMMU) converts logical addresses to physical addresses by the means of internal mapping [3]. An ESC provides 4GB logical address space. One telegram can read and write several slave devices arbitrarily distributed. The operating principle of FMMU is shown in Fig.2. Fig.3 is a mapping example of FMMU. It illustrates the functions of an FMMU configured to map 6 bits from logical address 0x14711.3 to 0x14712.0 to the physical register bits 0x0F01.1 to 0x0F01.6.

SyncManager is used to ensure the consistency and security of exchanging data between the EtherCAT master and a local application. It is configured by master station including communication direction and communication mode. Two operating modes are supported by SyncManagers: buffered mode and mailbox mode. The buffered mode allows both sides, EtherCAT master and local application, to access the communication buffer at any time. It is typically used for periodic process data. The mailbox mode implements a handshake mechanism for data exchange, so that data will not be lost. Each side will get access to the buffer only after the other side has finished its access. The mailbox mode is typically used for application layer protocols.

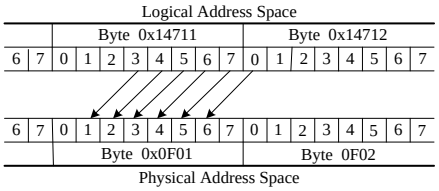

Fig. 3: FMMU mapping example

3. System Design and Implementation

3.1. The whole structure of system

The proposed system consists of slave stations and a master station which is a PC with standard Ethernet card. They are connected to perform a closed loop [4] shown in Fig.4. The master station sends commands to slave stations though Ethernet frames and takes the collected data from slave stations back to analyze and process.

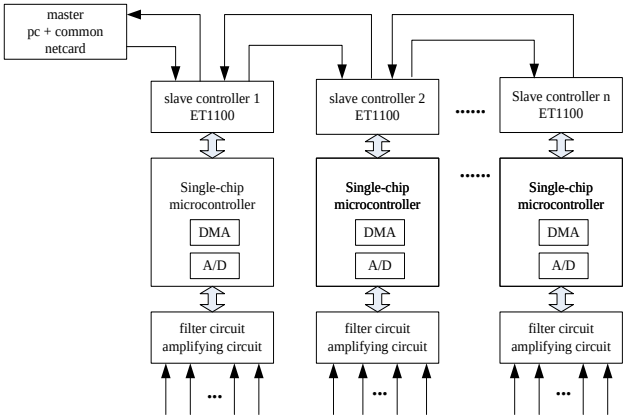

Fig. 4: The whole structure of system

3.2. Design of hardware circuit

Prior to access to Micro Controller Unit (MCU), the input signals should be filtered and amplified. The purpose of filter circuit is to improve capacity of resisting disturbance to prevent the outside interference signal and noise from affecting the wanted signal. Amplifying circuit is used to amplify weak input signals to proper value. Fig.5 shows the connections to MCU. Filter circuit is a one-order low pass filter which has inverting input. Its cut-off frequency is 1/ (2πRfC), 1K Hz. AD8250 is used as amplifier integrating three operational amplifiers inside. Its gain can be programmed digitally. Users can select from four kinds: 1, 2, 5, and 10. Differential inputs make the scope of common- mode voltage wide and 80dB common-mode rejection capability. The peripheral circuit is very simple. The combine of precise DC characteristic and high-speed ability makes it very suitable for data acquisition system. The output signals of amplifier enter into microcontroller and get access to ADC module though analog multiplexer.

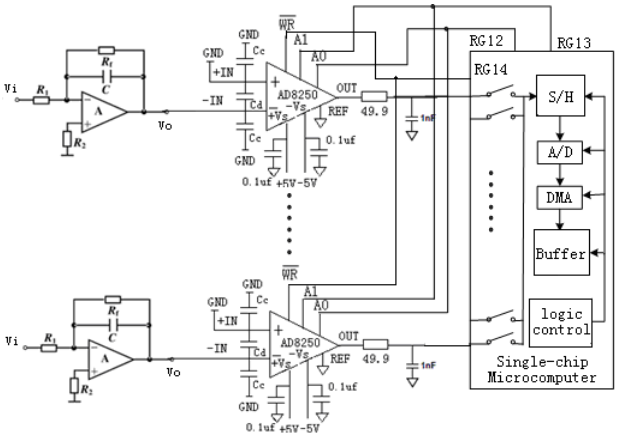

Fig. 5: Connections of MCU and peripheral circuits

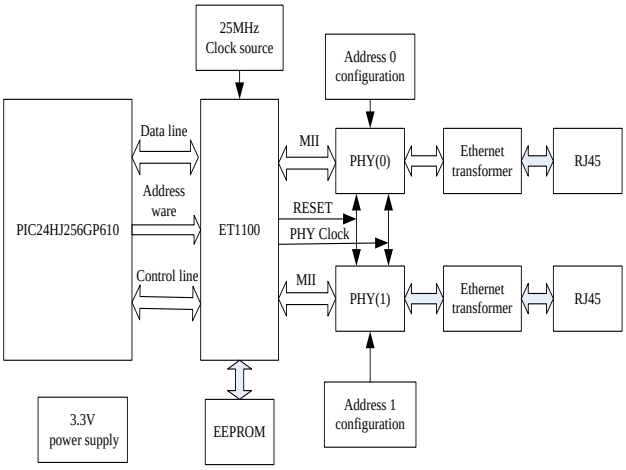

Fig. 6: Block diagram of interface circuit

The functions of slave station are achieved under the control of microcontroller. The interface circuit block diagram as we see in Fig.6 consists of EtherCAT slave controller ET1100, Single-chip Microcomputer Microchip PIC24HJ256GP610, physical layer chip Micrel KSZ8721BL, Ethernet transformer H1102, and RJ45 [5]. RJ45 is connected to network card though network cable. As microcontroller of application layer PIC24HJ256GP610 is connected to ESC via MCI interface. Their data line, address wire and control line are connected respectively. The PHY chips share a clock source and are linked to ESC via Medium

Independent Interface (MII).

The MCU completes functions of application layer and the control task. It reads data from ESC to control the peripheral devices and write required data to ESC for master station to read. The communication between master station and slave station is processed by ESC. PIC24HJ256GP610 is a Microchip's high-end 16-bit microcontroller with Harvard bus to improve the speed of executing commands [6]. The Analog-to-Digital Converter (ADC) inside is used to complete data acquisition with high accuracy and short delay. The DMA controller can store the digital data after ADC to dual-port SRAM rapidly until the buffer is full and then make an interrupt, so it can reach high efficiency. Fig.7 demonstrates its structure diagram. ADC is connected to channel 1 of DMA controller as a ready peripheral device. The data is transmitted to dual-port SRAM though a dedicated bus. Users can process data though the other port of SRAM.

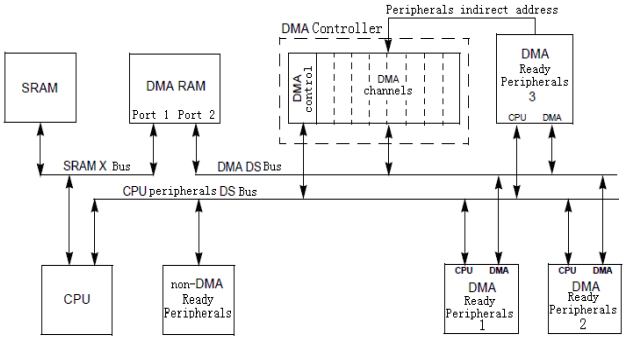

Fig. 7: Block diagram of DMA controller

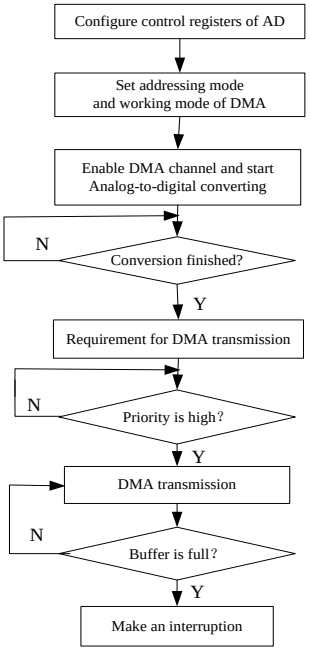

Fig. 8: Flow chart of data acquisition

3.3. Design of software

1) Software of slave station: The software of slave station is responsible for initialization of microcontroller, communication variables, EtherCAT slave controller and state machine. And it also used to complete state changes, communication of non periodic and process data to complete data acquisition. We can see the flow chart in Fig.8.

The working process of DMA is as followed: when the data conversion is finished, it will require for DMA transmission. The requirement will be arbitrated together with other requirements. If it has a high priority, it will be processed and start transmitting data at the next cycle. Otherwise this requirement will keep waiting until it has a high priority. The proposed design uses only one DMA channel, so the requirement can get response at any time. Then the data in ADCBUF0 (the collected data) will be read and written to expected address of DPSRAM. Register indirect addressing mode is adopted with DMA status registers DMA0STA and DMA0STB specifying initial offset address of main and assistant SDPRAM respectively. The reading and writing operations are completed within one instruction cycle without interruption. In the whole process, the DMA requirement is locked until transmission is finished. The transmission counter is monitored to make an interruption when the counter increased to an expected value to remind the microcontroller to process the latest collected data. Because of ping-pang mode is used, a single DMA channel can support two buffers of the same length. The microcontroller can process data of one buffer and load data to the other at the same time so as to achieve maximum data throughput. So the master station can collect large quantities of data from every slave station at one time to improve the working efficiency greatly.

2) Software of master station: The functions of master station are achieved by TwinCAT software with a real-time kernel running inside. The kernel is embedded in operation system with a higher priority to use CPU so as to achieve real-time communication [7]. The functions include initialization of network, communication

of periodic and non periodic data. In the proposed paper we develop user interface to display value and curves of collected data in VC++ environment through R3IO interface.

4. Experimental Results

Experiments have been done to evaluate the performance of the system. We can select the channels from sixteen channels to be used for collecting, shown in Fig.9. We select three of the channels and take the sine waveform which is generated from the generator as input signal. The period of the signal is 1 second and the amplitude is 1.5 volt. According to the picture, the waveforms are smooth, and the data points are distributed evenly, which demonstrate the stability and practicality the proposed system.

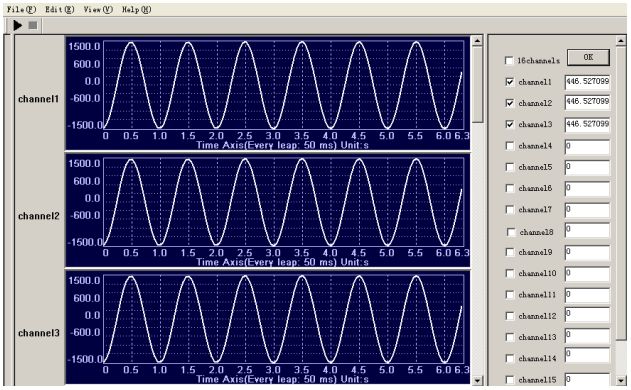

Fig. 9: Display of collected data

5. Conclusions

This paper focused on the application on mass data acquisition system of EtherCAT, which has been achieved in DMA mode. The system can be constructed easily and easy to extend with high reliability and stability. The efficiency and communication speed of data acquisition are improved greatly. Meanwhile we can configure the control registers to use non-DMA mode for gathering small quantities of data with little time. It can be controlled flexibly according to the requirement. The proposed system was successfully tested. It can be used in various applications that require high-speed real-time data acquisition.

6. Acknowledgment

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