

# A Digital Signal Processing System of Biphase Coded QCW Radar Based on FPGA

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**Abstract.** The biphase coded quasi-continuous wave(QCW) radar, which combines the advantages of both continuous wave (CW) radar and pulse Doppler (PD) radar, will be widely used in the land detecting filed in the near future. After building the model of transmitting and receiving signals of radar, the theoretical simulation of the digital signal processing system with Matlab is provided in this paper. Then the implementation of the system in FPGA is illustrated in detail. The system accomplishes the function of digital down converter (DDC), clutter suppression, pulse compression, range-gate permutation, Fast Fourier Transform (FFT) and so on, with the data streaming structure. Finally, the system testing proves that the output of practical system was consistent with the theoretical result of simulation.

**Keywords:** Biphase code; Quasi-continuous wave radar; Digital signal processing; FPGA

## 1. Introduction

Biphase codes are widely used in radar now because of good autocorrelation and thumbtack ambiguity function [1]. Pulse compression of biphase coded radar can resolve the conflicts between through range and range resolution and enhance the capacity against the wide-band signals such as land clutter. Biphase coded continuous wave (CW) multistatic Radar is described in [2]. EH.Khan and D.K.Mitchwell put forward the conception of quasi-continuous wave radar in [3], however, they only discuss the LFM signals. We obtain the biphase coded quasi-continuous wave (QCW) radar which has the advantage both CW radar and pulse Doppler (PD) radar by using biphase coded signals in quasi-continuous wave radar. It not only solves the problem of transmit leakage of CW radar, but also overcomes the PD radar's shortcoming of high peak value. Owing to its high resolution of range and frequency, good anti-jamming capability and the property of low probability of intercept, the biphase coded QCW radar meets the development trends of ground reconnaissance radar.

The full digitalization of the signal processing system of radar makes it more flexible and steady with higher accuracy. The techniques of digital signal processing such as digital down converter (DDC), digital filter, fast Fourier transform (FFT) and so on, also contribute a great deal to the signal processing of radar [4]. With the development of large scale integrated circuit, FPGA is more suitable for high-speed, real-time, and parallel digital signal processing. FPGA plays an important role in radar signal processing [5][6][7]. A digital signal processing system for the biphase coded QCW radar based on FPGA is simulated and illustrated in detail in this paper. The experimental results prove that the system can estimate the power spectral density of targets effectively in real time.

The rest of the paper is organized as follows. The transmitting and receiving waves of biphase coded QCW radar are analyzed in section II. Section III simulates the signal processing system of radar with

Matlab. The implementation of signal processing system in FPGA is described in section IV. Section V offers the practical testing results. Finally, in section VI the conclusion is given.

## 2. Transmitting and Receiving Waves of Biphase Coded QCW Radar

Suppose  $x(t)$  is pseudo random sequence with amplitude chosen from  $\{1,-1\}$  and  $u(t)$  is rectangular pulse with width of  $T_l$ . Thereby, the base-band signal  $b(t)$  is expressed as:

$$b(t) = k \sum_{m=0}^{N-1} u(t - mT_r) \cdot \sum_{n=0}^{P-1} v(t - nT_p) x(t) \quad (1)$$

$$= \frac{1}{\sqrt{NPT_p}} \sum_{m=0}^{N-1} \sum_{n=0}^{P-1} u(t - mT_r) v(t - nT_p) x(t) \quad (2)$$

$$\text{Where } v(t) = \begin{cases} 1 & 0 \leq t < T_p \\ 0 & \text{others} \end{cases}, \quad (3)$$

$T_r$  is pulse repetition period,  $N$  is pulse repetition times,  $T_p$  is subcode duration.

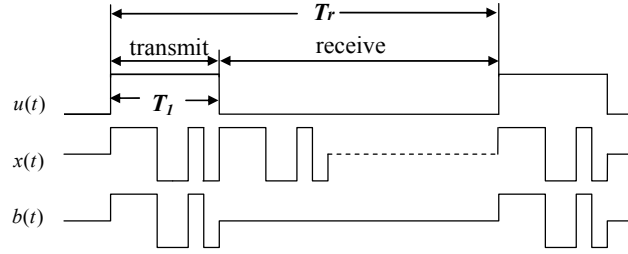


Fig.1. The base-band signal

Suppose  $T_1$  is the transmitting time and  $T_2$  is the receiving time (usually  $T_1 < T_2$ ), so the pulse repetition period is

$$T_r = T_1 + T_2 \quad (4)$$

The wave like  $b(t)$  as shown in Fig.1 can be called QCW wave, and the transmitting wave of Biphase coded QCW radar can be written as:

$$S(t) = \frac{1}{\sqrt{NPT_p}} \sum_{m=0}^{N-1} \sum_{n=0}^{P-1} x(t) \cdot u(t - m \cdot T_r) \cdot v(t - nT_p) \cdot \cos[2\pi f_0 t + \varphi_0] \quad (5)$$

Where  $f_0$  is the frequency of carrier wave and  $\varphi_0$  is the initial phase. So the target echo (single target) is

$$R(t) = A_r \sum_{m=0}^{N-1} \sum_{n=0}^{P-1} x(t) \cdot u(t - m \cdot T_r - \tau) \cdot v(t - nT_p - \tau) \times \cos[2\pi f_0(t - \tau) + 2\pi f_d t + \varphi_0] \quad (6)$$

Where  $\tau$  is the delay time and  $f_d$  is Doppler frequency.

Comparing with the transmitting wave, the receiving wave has two new parameters,  $\tau$  and  $f_d$ , which mean the rang and the speed of target. We can obtain them by digital signal processing.

## 3. Simulation of Signal Processing System

The processing flow chart is shown in Fig.2. Firstly, we sampling the received intermediate-frequency signal with high-speed ADC and converts it down to base-band digital signal using DDC. At this time, we get in-phase (I) and quadrature-phase (Q) channel base-band signals. Secondly, the two channels of base-band signals are parallelly processed with clutter suppression (CS), pulse compression (PC), range-gate permutation and Doppler filtering. Finally, we transmit all the data to DSPs after FFT for the two branches of signals. The DSPs gives the detection result through CFAR. We only discuss the section of processing in FPGA in this paper.

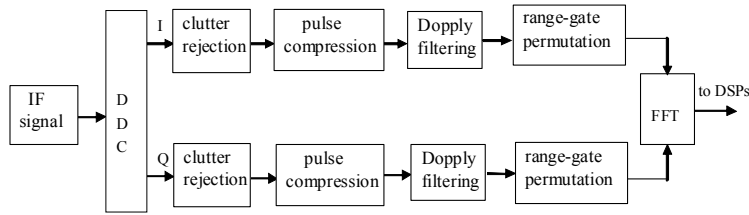


Fig.2. Processing flow chart of Biphase coded QCW radar

Here we simulate the processing system in Matlab with the parameters in Table I. Biphase codes are Barker codes with length of 13 bits. There are two targets in the radar echo. The one with Doppler frequency 0KHz is located in 200th range gate, the other with Doppler frequency -1KHz is located in 20th range-gate.

Table 1. System Parameters

Parameter	Value	Unit
ADC sampling frequency	80	MHz
intermediate frequency	60	MHz
Barker codes	1 1 1 1 1 -1 -1 1 1 -1 1 -1 1	-
bit rate	10	MHz
transmitting time	1.3	us
receiving time	50.7	us
duty ratio of transmitting wave	1:40	-
pulse repetition frequency	19.23	KHz
pulse repetition times	2560	-
range bins	350	-
Doppler banks	1024	-
signal to noise ratio	-8	dB

Fig.3 shows the IF signal of a pulse repetition period. We can see that there are two targets in the radar echo. The noise is so strong that the sinusoidal signal modulated by Barker codes is almost flooded into the noise. What's more, the phase information of the biphase codes in IF signal is damaged to some extent.

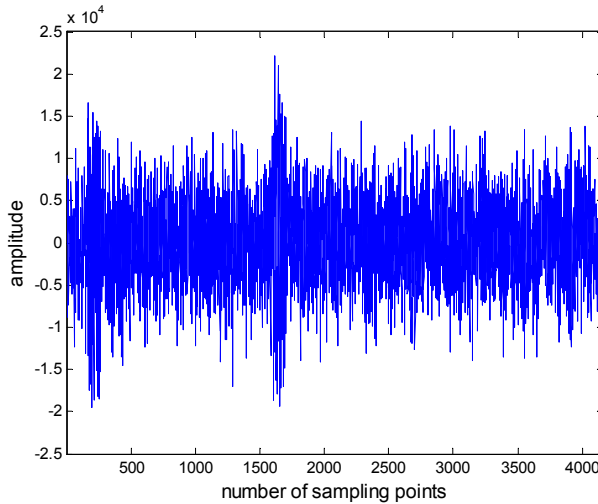


Fig.3. IF signal of a pulse repetition period

### 3.1. DDC and Decimation

In order to convert IF signals to base-band signals, analog mixing and analog filtering is the traditional method. So we get two base-band signals by two ADCs. However, the orthogonality is always unsatisfactory by this way. But DDC can solve the problem easily. DDC samples the IF signals directly by only one ADC and multiply it by local digital carrier. Eventually, two base-band signals are obtained by getting through the low pass filter. The low pass filter is designed according to the parameters in Table II.

Table 2. Low Pass Filter Parameters

Parameter	Value	Unit
sampling frequency	80	MHz
pass band frequency	10	MHz
pass band ripple	0.1	dB
cut-off frequency	12	MHz
stop band attenuation	45	dB

Fig.4 shows the base-band signal after DDC and decimation.

Then the bit rate changes from 80MHz to 10MHz. The fixed ground feature only exists in in-phase channel, but moving target exists in both in-phase and quadrature-phase channel. And the amplitude of moving target signal varies in different pulse repetition periods, obeying the sine function.

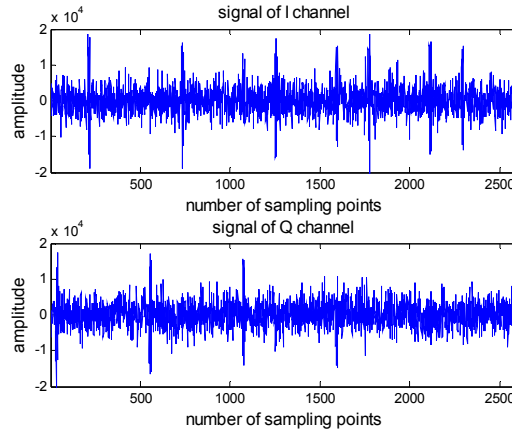


Fig.4. Base-band signals after DDC and decimation

### 3.2. Clutter Suppression

The fixed ground feature reflection is always much stronger than moving target in ground reconnaissance radar operating environment. Strong land clutter reflection makes it difficult to detect the weak small targets under the strong clutter background. Fortunately, the spectrum component of the fixed ground feature is only significant around zero frequency [8]. So clutter suppression aims to weaken fixed ground feature reflection in the frequency domain.

The amplitude-frequency characteristic of single and double delay for cancellation is not so cliffy that we can use the delay line with feedback instead, whose system function is

$$H(z) = \frac{1 - z^{-1}}{1 - 15z^{-1}/16} \quad (7)$$

The system function in (7) represents an IIR filter. The filtering is carried out between pulse repetition periods. In other words, the sampling frequency of the IIR filter is 19.23KHz.

As shown in Fig.5, fixed features have been disappeared after clutter suppression, and the moving target is still in both in-phase and quadrature-phase channel.

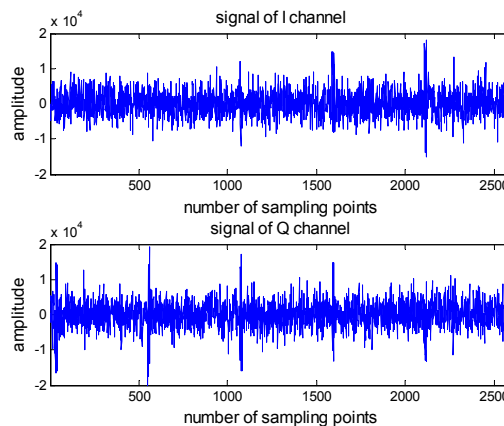


Fig.5. Signals after clutter suppression

### 3.3. Pulse Compression and Sidelobe Suppression

Pulse compression, producing narrow pulse signal after the base-band signals pass through the matched filter, improves the detection ability of radar. However, the sidelobe of big targets is always stronger than the main lobe of weak targets when the biphasic code signals carry out matched filtering. So it makes sidelobe suppression necessary.

Matched filtering cascading weighting network and mismatch filtering are the two main methods of sidelobe suppression and we choose the second one. A mismatch filter with length of 39 is designed for Barker codes based on LS arithmetic [9][10]. Table III shows the material parameters of the mismatch filter.

Table3. Mismatch Filter Parameters

Parameter	Value	Unit
Peak Sidelobe Level (PSL)	-38.47	dB
Integrated Sidelobe Level (ISL)	-30.030	dB
Loss in ProcessGain(LPG)	0.20	dB

Fig.6 shows the base-band signals after pulse compression. We can see that the biphasic codes are compressed into a single peak. It improves the range resolution enormously. Obviously, the signal to noise ratio (SNR) of the base-band signals is improved at the same time.

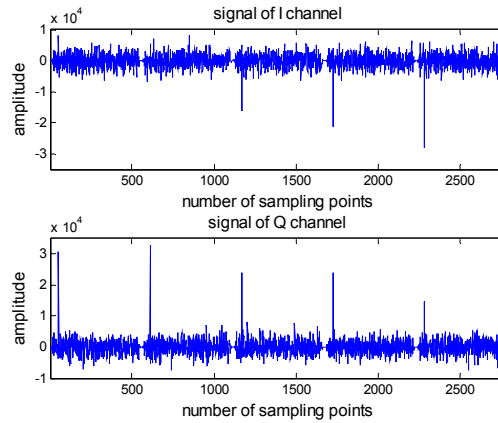


Fig.6. Signals after pulse compression

### 3.4. Range-gate Permutation and FFT

A pulse repetition period can be divided into many range gates. Radar echo signal is arranged to a two-dimension array by range-gate permutation, according to the pulse repetition period and the sequence number of range gates. The echo signal is arranged in rows in the same pulse repetition period and arranged in columns in the same range gate. So Doppler filtering and FFT process echo data in columns.

Doppler filter is a low pass filter, removing the frequency out of the detection frequency range. The low pass filter is designed according to the parameters in table IV.

Table 4. Doppler Filter Parameters

Parameter	Value	Unit
sampling frequency	19.23	KHz
pass band frequency	2.4	KHz
pass band ripple	0.1	dB
cut-off frequency	3	KHz
stop band attenuation	45	dB

Fig.7 shows the in-phase and quadrature-phase channel of the No.20 range gate signals. The peaks produced by pulse compression in the No.20 range gate are arranged into an array. We can see that the two channels of signals contain Doppler information of the moving target.

FFT estimates the power spectrum density with Welch arithmetic. We carry out 4 times 1024-point FFT operation by sliding window. The number of overlap data is 512. Sequentially we get the final result by averaging the four outputs of FFT.

Fig.8 shows the average normalized PSD of No.20 range gate in dB. We obtain a maximum value of normalized PSD at 54th spectral line. That is:

$$(54 - 1) * 19.23/1024 = 0.995\text{KHz} \quad (8)$$

At the beginning, we set the Doppler frequency of the moving target as 1KHz. So we obtain the speed correctly.

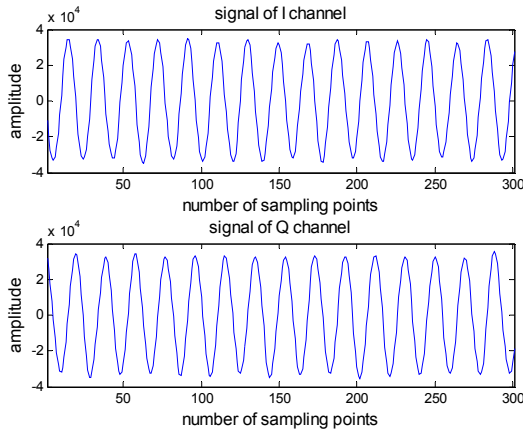


Fig.7. Signals of No.20 range gate for FFT

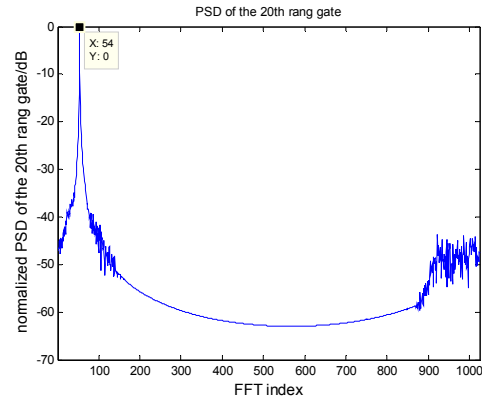


Fig.8. Average normalized PSD of No.20 range gate

#### 4. Implementation of Signal Processing System in FPGA

The flow chart of the implementation of signal processing system in FPGA is shown in Fig.9. EP3SEL110 produced by Altera Corporation is taken as the main processing chip. Inputs and outputs of every module of the system are signed fixed point number with width of 16 bits.

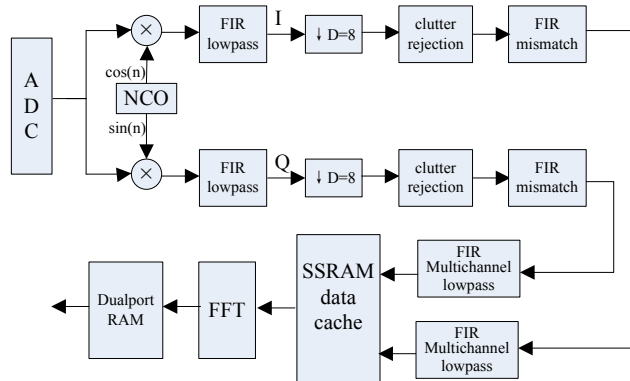


Fig.9. Flow chart of Implementation in FPGA

LTC2208, which is produced by Linear Technology Corporation with a resolution of 16 bits, is used as the ADC chip. The sampling frequency of ADC is 80MHz. The NCO module outputs the cosine and sinusoidal signals with 20MHz frequency. But the NCO working frequency is 80MHz. Then we multiply ADC data by NCO data follow the structure in Fig.9. So DDC is completed when I and Q channel signals get through the low pass filter. The base-band data rate is 10MHz after decimation.

The structure of clutter suppression module is shown in Fig.10. It is an IIR filter. The base-band data delays a pulse repetition period to feed back to calculate the output, so a  $507 \times 32\text{b}$  dual-port RAM is needed to cache base-band data.

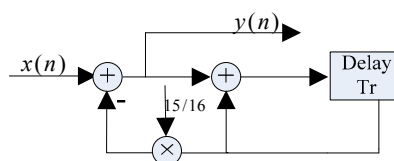


Fig.10. The structure of clutter suppression module

The mismatch filter is a FIR filter whose working clock is 10MHz. The number of channels of the Doppler filter is the same as range bins and we use 350 range gates. The Doppler filter gives out the sampling value of Doppler data of different range gates. So the Doppler filter equals 350 parallel FIR filters with 19.23KHz working clock frequency. When FPGA puts the data into SSRAM, the writing address is

$$SSRAM \text{ write address} = i * 2560 + j \tag{9}$$

where  $i$  is the sequence number of the pulse repetition period and  $j$  is the sequence number of range gate.

We use two 1M×36b SSRAMs to cache the 2560 periods of data. Ping-pong operation is available between two SSRAMs. All the data can be read out from SSRAM orderly when FFT is computing. To realize the sliding window, a finite state machine is applied in FPGA. Finally the modulus of FFT is transferred to DSPs through dual-port RAM.

## 5. System Testing

SignalTap in software Quartus II, which is the embedded logic analyzer in FPGA, can display outputs of every module on line in real time. We input the IF signals with parameters as follows: intermediate frequency is 60MHz; the one target with Doppler frequency 0KHz is located in 200th range gate, the other with Doppler frequency -1KHz is located in 20th range gate; SNR is -8dB. The output signals of key modules are shown in Fig.11.

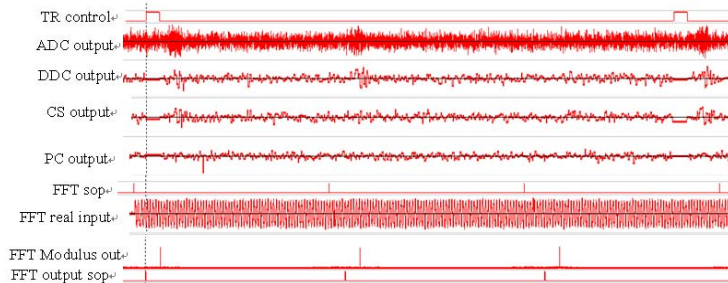


Fig.11. The output signals of key module

As shown in Fig.11, when TR control signal is low, the signal processing system works. ADC is working all the time. DDC outputs the base-band signal and we can see the outline of the biphase codes among them. Then the biphase codes of fixed features are eliminated by clutter suppression. Pulse compression changes the biphase codes into a single peak. Regular sinusoidal signal appears in No.20 rang gate when the data are read out from SSRAM. There is a peak in 1024-point FFT output, which indicates the speed of the moving target.

We can get a detection result after accumulating data for 2560 repetition periods. The final output of 350 range gates, which is the logarithm of the normalized modulus of FFT, is shown in Fig.12. From the three-dimension figure of range and speed, we obtain a maximum value of normalized PSD in 20th rang gate, 54th spectral line.

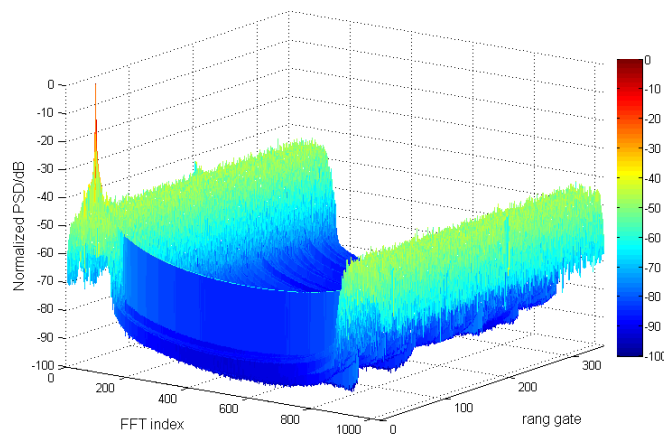


Fig.12. A detection result

## 6. Conclusion

After building the model of transmitting and receiving signals, the theoretical simulation result of digital signal processing system for Biphase coded QCW radar with Matlab is provided in this paper. Then the implementation of the system in FPGA, which has accomplished the function of DDC, clutter suppression, pulse compression, range-gate permutation, FFT and so on, with the data streaming structure, is illustrated. Finally, the system testing proves that the output of practical system was consistent with the theoretical result of simulation. The experimental results prove that the system can estimate the power spectral density of targets effectively in real time. The high-speed, real-time, and parallel digital signal processing in FPGA reduces the heavy burdens of DSPs tremendously.

## 7. Acknowledgment

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## 8. References

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