

# An Ultra-low Power Voltage Reference for Passive UHF RFID Tag

Jinpeng Shen, Xin'an Wang<sup>+</sup>, Shan Liu and Jinfeng Huang

The Key Laboratory of Integrated Microsystems  
Peking University Shenzhen Graduate School

**Abstract.** This paper presents an ultra-low power voltage reference for passive UHF RFID tag. The voltage reference uses the peaking current source to generate a temperature-independent reference voltage while retaining circuit simplicity. Simulation results show that temperature coefficient of the voltage reference is 125ppm/°C when temperature ranges from -20°C to 60°C, while line regulation is 1.7%/V when the supply voltage ranges from 1.1v to 3v. The current consumption is only 150nA. The circuit layout occupies 114  $\mu\text{m} \times 114 \mu\text{m}$ . The whole tag chip is implemented in TSMC 0.18  $\mu\text{m}$  CMOS process with a die size of 620 $\times$ 610  $\mu\text{m}^2$ . Measurement results show that at a 2v supply voltage, the output reference voltage rises up to a stable 960mv voltage level in 100  $\mu\text{s}$ .

**Keywords:** UHF RFID tag, voltage reference, ultra-low power, peaking current mirror

## 1. Introduction

Nowadays Radio Frequency Identification (RFID) tags operating in UHF band are showing a wide prospect of applications, including intelligent transportation systems, asset tracking, supply-chain management, logistics, and many other areas [1-4]. The operating range of the UHF RFID system is highly dependent the tag's power consumption [5], so it is very important to design ultra-low power circuits for passive tag to achieve a longer communication distance.

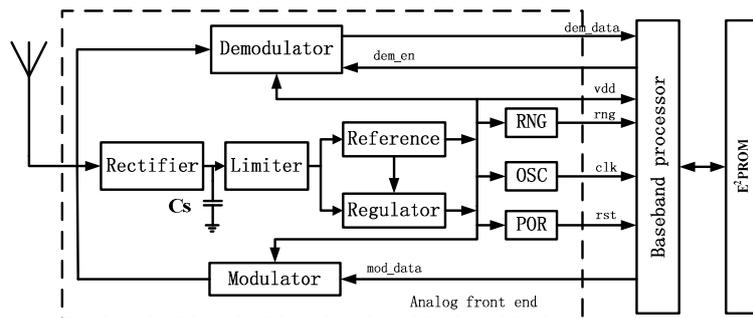


Fig. 1: System architecture of a passive UHF RFID tag.

Fig.1 shows the system architecture of a passive UHF RFID tag, which includes a RF/analog front-end, a baseband processor and an EEPROM memory. The passive tag power is harvested from RF energy through the rectifier. Due to the huge variations of the incoming RF power, the rectifier output voltage has a large variation (1.1v~3v in our system). Hence, a reference circuit is used to generate a stable voltage reference and it must be able to tolerate this large variation. Conventional band-gap reference circuit [6] is not suitable for low-voltage design. Several sub-1v voltage reference circuits are reported in [7, 8], but they don't fit the

<sup>+</sup> Corresponding author. Tel.: +0755-26035359; fax: +0755-26035374.  
E-mail address: wangxa@szpku.edu.cn.

RFID tag because of their large power consumption. In this paper, we propose a novel voltage reference circuit using peaking current source to generate stable reference voltage. This circuit is less complex than previous approaches<sup>[6-8]</sup> and can meet the low-power, low-voltage requirement.

## 2. Voltage reference design

The peaking current source<sup>[9, 10]</sup> has been recognised as a useful low-current reference. This work exploits the peaking source to realise a low-power voltage reference. Fig.2 depicts the proposed voltage reference circuit. The peaking current source is composed of the elements Q1, Q2 and R1. The elements MP3 and MP4 are connected in a current mirror, which serves for realising the function of self-biasing. The MP3, MP4 mirror is designed that the collector current of Q1 and Q2 operate in the peaking relation. Then the voltage across R1 is proportional to the absolute temperature (PTAT). Thus, the resistor ratio R3/R1 can be used to compensate the temperature variation of the base-emitter voltage of Q3. A temperature independent reference voltage output,  $V_{ref}$ , is therefore obtained. The detailed analysis is as follows.

Ignoring base current, the collector currents of Q1 and Q2 can be given by

$$I_1 = I_{S1} \exp\left(\frac{V_{BE1}}{V_T}\right), \quad (1)$$

$$I_2 = I_{S2} \exp\left(\frac{V_{BE2}}{V_T}\right), \quad (2)$$

where  $I_{S1}$  and  $I_{S2}$  are the reverse saturation currents of Q1 and Q2 respectively,  $V_T$  is the thermal voltage,  $V_{BE1}$  and  $V_{BE2}$  are the base-emitter voltages of Q1 and Q2 respectively.

The relation between the two collector currents, therefore, is

$$\begin{aligned} I_1 &= I_2 \frac{I_{S1}}{I_{S2}} \exp\left(\frac{V_{BE1} - V_{BE2}}{V_T}\right) \\ &= I_2 N \exp\left(\frac{V_{BE1} - V_{BE2}}{V_T}\right), \end{aligned} \quad (3)$$

where  $N$  is the emitter area ratio between Q1 and Q2.

The difference between two base-emitter voltages of Q1 and Q2 can be expressed as

$$V_{BE1} - V_{BE2} = -I_2 R_1, \quad (4)$$

substituting Equation (4) into Equation (3), we obtain

$$I_1 = I_2 N \exp\left(-\frac{I_2 R_1}{V_T}\right). \quad (5)$$

The peaking current source is designed such that  $I_1$  is at its peaking value. It can be achieved by zeroing the derivative of  $I_1$  with respect to  $I_2$  using Equation (5), yielding the following design condition

$$I_2 R_1 = V_T. \quad (6)$$

If the condition is satisfied, then the collector currents of Q1 and Q2 are related by

$$I_1 = I_2 N e^{-1}. \quad (7)$$

Hence, the self-biasing mirror constituted by MP3 and MP4 is designed to make  $I_1$  and  $I_2$  satisfy the relation in Equation (7).

In our design, we choose  $N = 2$ , then setting  $K_3 = K_4 * 2 * e^{-1}$  will make the peaking condition satisfied ( $K_3, K_4$  are the width to length ratios of MP3 and MP4 respectively). If setting  $K_4 = K_5$ , we will get

$$I_2 = I_3 \quad (8)$$

So the output reference voltage can be written as

$$V_{ref} = V_{BE3} + I_3 R_3 = V_{BE3} + \frac{R_3}{R_1} V_T \quad (9)$$

In Equation (9),  $V_T$  has a positive temperature coefficient while  $V_{BE3}$  has a negative one. So  $V_{ref}$  can be designed to be temperature independent by carefully choosing the value of  $R_3$  and  $R_1$ . Fig.3 (a) shows simulation results of  $V_{ref}$  as a function of temperature. The temperature coefficient of the voltage reference is 125ppm/°C when temperature ranges from -20°C to 60°C.

In the reference circuit, MN6 is used to keep collector voltage of Q2 stable under large variation of the supply voltage, which will reduce the impact of the Early effect. According to [11], considering the Early effect, the collector current of Q1 is given by

$$I_1 = I_{S1} \left(1 + \frac{V_{CE1}}{V_A}\right) \exp\left(\frac{V_{BE1}}{V_T}\right), \quad (10)$$

where  $V_{CE}$  is the collector-emitter voltage,  $V_A$  is the Early voltage.

If MN6 is not used, the collector voltage of Q1 will follow the variation of the supply voltage (1.1v to 3v in our design), which can induce a large variation of  $V_{CE1}$ . According to Equation (10),  $I_1$  varies a lot with the supply voltage, causing a large variation of  $V_{ref}$ . So to minimum this variation of  $V_{ref}$ , MN6 is adopted. The gate voltage of MN6 is relatively stable, which will make the collector voltage of Q1 stable. Thus,  $V_{ref}$  varies little with the supply voltage. Fig.3 (a) shows the simulation results of  $V_{ref}$  as a function of supply voltage, the line regulation is 1.7%/V when the supply voltage ranges from 1.1v to 3v.

MN1, MN2, MN3, MP1, and MP2 constitute a start-up circuit without static power consumption. When the circuit is powered on, node "A" firstly becomes high to turn on MN3, which will inject pulse current through MP3 to set the circuit to the right operating point. Then node "B" turns high, which will turn on MN1. Thus, node "A" becomes low and MN3 is shut down.

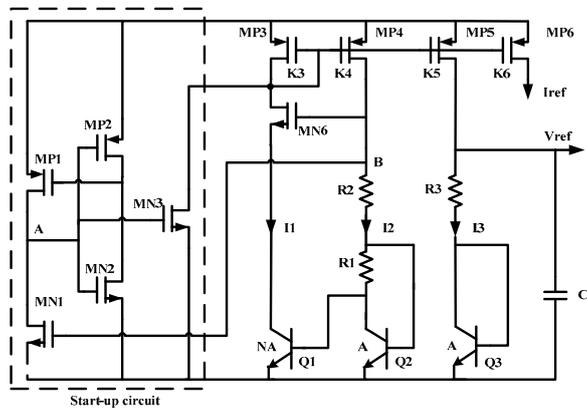


Fig. 2: Schematic of the proposed reference

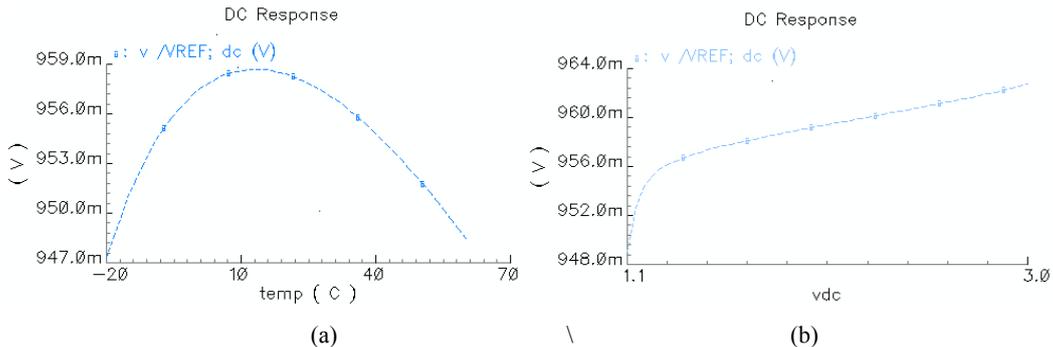


Fig. 3:  $V_{ref}$  as a function of (a) temperature and (b) supply voltage

### 3. Experiment results

Layout of the voltage reference occupies  $114\ \mu\text{m} \times 114\ \mu\text{m}$ . Fig.4 is the post simulation results, considering the process variations of MOSFET, BJT and resistor, the output reference voltage ranges from 934mv to 975mv in the condition of supply voltage varying from 1.1v to 3v while temperature from  $-20^\circ\text{C}$  to  $60^\circ\text{C}$ . The start-up time is less than  $200\ \mu\text{s}$  and the current consumption is only 150nA. The whole tag chip is implemented in TSMC  $0.18\ \mu\text{m}$  CMOS process with a die size of  $620 \times 610\ \mu\text{m}^2$ , as Fig.5 shows. Fig.6 is the measured results of the voltage reference. It shows that at a 2v supply voltage, the output reference voltage rises up to a stable 960mv voltage level in  $100\ \mu\text{s}$ .

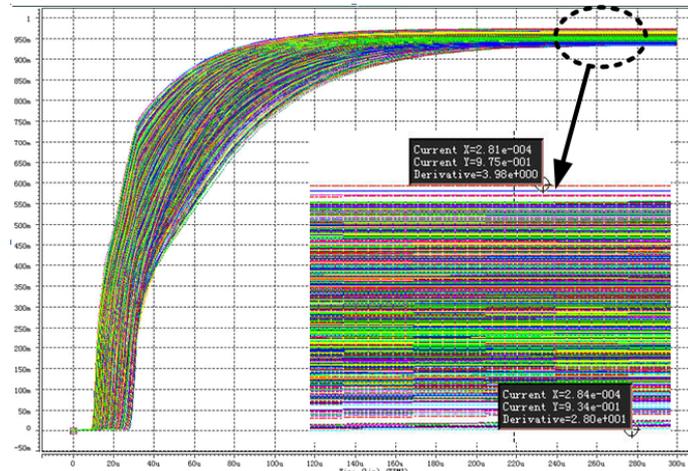


Fig. 4: Post simulation results of the proposed voltage reference

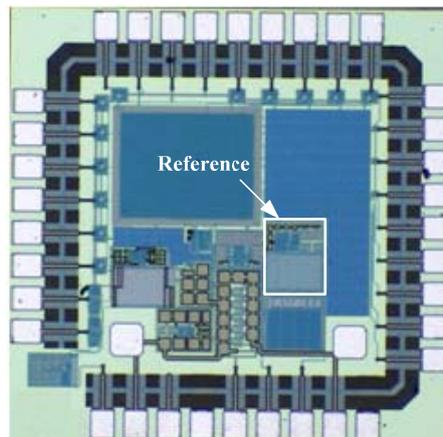


Fig. 5: Die photo of the tag chip

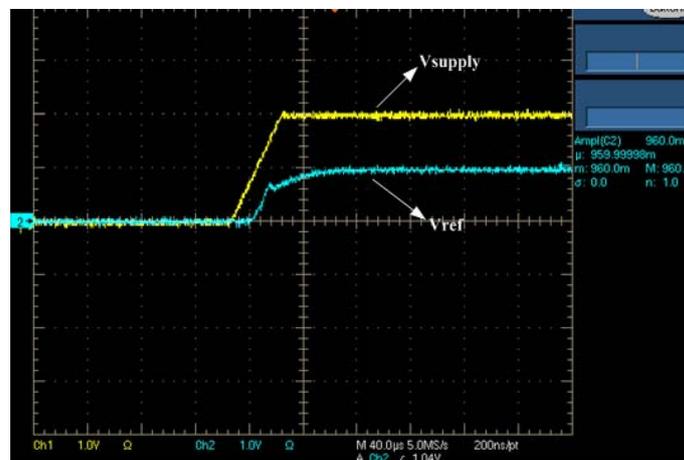


Fig. 6: Measured results of voltage reference

## 4. Conclusions

This paper presents an ultra-low power voltage reference for passive UHF RFID tag. The voltage reference adopts the peaking current source to generate a temperature-independent reference voltage while retaining circuit simplicity. Simulation results show that the circuit has small process, voltage and temperature coefficient. The current consumption is only 150nA. The voltage reference circuit is less complex than previous approaches and can meet the low-power, low-voltage requirement.

## 5. Acknowledgements

The authors would like to thank Prof. Wang Xin'an for his help. This research was supported by Shenzhen Key Laboratory Development Project (NO. CXB201104210007A).

## 6. References

- [1] Karthaus U, Fischer M. Fully integrated passive UHF RFID transponder IC with 16.7uW minimum RF input power. *IEEE J Solid-State Circuits*, 2003, 38(10): 1602-1608.
- [2] Daniel M. Dobkin. *The RF in RFID: Passive UHF RFID in Practice*. Newnes Press, 2007.
- [3] K. Finkenzerler. *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification*, 2nd edition. Wiley Press, 2003.
- [4] Raymond E. Barnett, Jin Liu, and Steve Lazar. A RF to DC Voltage Conversion Model for Multi-Stage Rectifiers in UHF RFID Transponders. *IEEE Journal of Solid-State Circuits*, 2009, 44(2): 354-370.
- [5] G. D. Vita and G. Iannaccone. Design criteria for the RF section of UHF and microwave passive RFID transponders. *IEEE Trans Microwave Theory Tech*, 2005, 53(9): 2978-2990.
- [6] Yueming Jiang and Edward K. F. Lee. A 1.2V Bandgap Reference Based on Transimpedance Amplifier. *IEEE International Symposium on Circuits and Systems*. 2000, pp. 261-264.
- [7] Ka Nang Leung and Philip K. T. Mok. A sub-1-V 15-ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device. *IEEE Journal of Solid-State Circuits*, 2002, 37(4): 526-530.
- [8] Di Naro, G., Lombardo, G., Paolino, C., and Lullo, G. A Low-Power Fully-Mosfet Voltage Reference Generator for 90nm CMOS Technology. *IEEE International Conference on Integrated Circuit Design and Technology*. 2006, pp. 1-4.
- [9] Kerns, D.V. Optimization of the peaking current source. *IEEE Journal of Solid-State Circuits*, 1986, 21(4): 587-590.
- [10] Kerns, D.V. Enhanced peaking current reference. *IEEE Journal of Solid-State Circuits*, 1988, 23(3): 869-872.
- [11] J.M. Early. Effects of space-charge layer widening in junction transistors. *Proc. IRE*, 1952, 40(11): 1401-1406.