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Design of Low Power Low Noise High quality Factor Active Inductor Based Impedance Matching Network for Low Noise Amplifier

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Abstract. This paper presents a low power tunable active inductor suitable for designing impedance matching network for Low noise amplifier. The active inductor circuit uses differential MOS configuration as positive transconductor and PMOS cascode structure as negative transconductor of gyrator structure toincrease the quality factor and to reduce the noise voltage. Also, this structure provides possible negative resistance to reduce the inductor loss with wide inductive bandwidth and high resonance frequency. The designed active inductor is used for matching the input impedance of the low noise amplifier for low power applications. The designed active inductor and Low noise amplifier are simulated in 180nm CMOS process using HSPICE simulation tool. Simulation results of the active inductor shows an inductive bandwidth from 1.5MHz to 7.94 GHz and the inductance value ranges from 125nH to 1530nH respectively. The tunable range of the active inductor varies from 3.9 GHz to 12.3 GHz. It has less noise voltage of 9nV/√Hz and consumes less power consumption of 0.6mW. The Low noise amplifier achieves the gain of 18dB, low noise figure of 3.5dB and consumes low power of 7mW.

Keywords: Active inductor, Quality factor, Centre frequency tuning, PMOS cascode pair, tuning range, low power design.

1. Introduction

The rapid growth of RF systems has led to the demand of low power and compact transceivers for wireless communication applications. Low noise amplifier (LNA) is the first block of the receiver to amplify the received signal with little noise. To prevent the reflections of the incoming signal between antenna and LNA, the input impedance of the LNA needs to be matched to the antenna impedance. In the same way, the output impedance of LNA should be matched to the load impedance for maximum power transfer. To perform this, matching networks are needed at the input and output side of LNA as shown in Fig.1. LNAs can be designed using active inductors [1]. Active inductors can be used in the input matching network or at the load side [2]. There are four different input matching techniques used in the design of narrow band CMOS LNA are discussed in [3], they are SID, PLC, SL and PL methods.

Inductors play a vital role in the design of impedance matching networks. On-chip spiral inductors can be used for designing matching circuits. Though the on-chip spiral inductors are good passive devices, it is difficult to realize it for larger inductance values, high quality factor and smaller chip area [4]. Active inductors, on the other hand, provide large inductance value with high resonance frequency, high quality factor, small chip area and wide range of tuning ability [5]. There are several techniques for designing tunable active inductor using gyrator circuit [6]. However, each one of them differs by only one or a few of the desirable specifications such as compactness, low voltage operation, wide inductance band, high quality factor, low power consumption, high dynamic range, low noise and tunability.

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This paper discusses the design of active inductor to achieve high resonance frequency, better tuning capability less noise and low power dissipation which is suitable for designing low power and low noise input matching networks for LNA design.

Section II briefly describes the design of proposed active inductor. Section III describes design of LNA with input matching network using active inductor. The simulation results and the discussions are presented in Section IV and the concluding remarks are given in Section V.

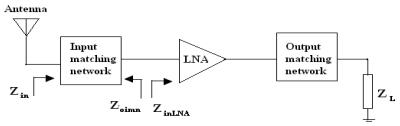
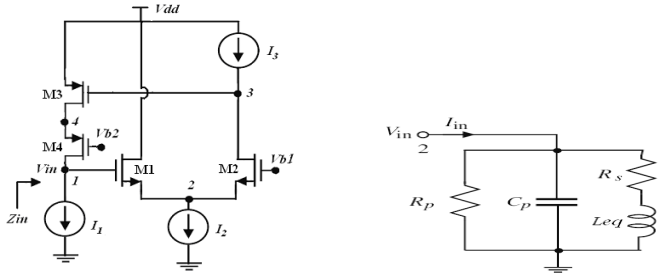


Fig. 1: Block of diagram of LNA with input and output matching networks

2. Design of Proposed Active Inductor

The proposed active inductor is realized using gyrator-C topology [5] is shown in Fig. 2(a). It consists of differential pair m1 and m2 which represents the positive transconductor G_{m1} between the input (node 1) and the output (node 3). The cascode pair m3 and m4 represents the negative transconductor $-G_{m2}$ between the input (node 3) and the output (node 1). Thus the G_{m1} and $-G_{m2}$ forms the gyrator which converts the parasitic capacitance C_3 at node 3 to an equivalent inductance Leq $=C_3/G_{m1}G_{m2}$. It is realized that, at frequencies below the self resonance, the simulated input impedance Z_{in} is equivalent to the passive circuit as shown in Fig. 2(b).



(a) (b)

Fig. 2: Circuit diagram of proposed single ended active inductor and its passive equivalent circuit

The differential configuration of G_{m1} makes the proposed active inductor, less sensitive to noise and interference. The PMOS cascode structure of negative transconductor $-G_{m2}$, led to possible negative resistance in series with the equivalent inductor to compensate the inductor loss. Thereby, enhances the quality factor of the active inductor. Also, the cascode structure provides frequency range expansion by lowering the lower bound of the frequency range, thus increases the inductive bandwidth. The p-channel transistors are preferred for cascode structure as they have low noise and they can be placed in separate n-wells, thus eliminating the non- linear body effect [6]. Thus, the combination of the differential configuration of Gm_1 and cascode configuration of $-Gm_2$ offers high inductive bandwidth, high resonance frequency and less noise.

The equivalent input impedance Z_{in}, can be obtained from the small signal analysis of the active inductor and using the equivalence $s^3 = -\omega^2 s$ [7] and $G= gm_1+gm_2+g_2$, it is given as,

$$Zin(s) \approx \frac{\frac{sg_4}{C1} + \frac{g_3 g_4}{C1C3}}{S^2 + s\left[\frac{g_1}{C_1} + \frac{g_1 g_3 C_2}{GC_1C_3} + \frac{g_3}{C_3} - \frac{\omega^2 C_2}{G}\right] g4 + \frac{gm_1 gm_2 gm_3 gm_4 + g_1 G g_3 [gm_4 + g_4]}{GC_1C_3}} \quad (1)$$

The format of Z_{in} shows that it is equivalent to an RLC network, as shown in Fig. 2(b). The‘s’ term in the numerator indicates the equivalent inductance and the real term indicates a resistor in series with the inductor. From equation (1), L_{eq} and R_s can be written as,

$$Leq = \frac{g_4 G C_3}{gm_1 gm_2 gm_3 gm_4 + g_1 G g_3 [gm_4 + g_4]} \quad (2)$$

$$R_S = \frac{G g_3 g_4}{g_{m1} g_{m2} g_{m3} g_{m4} + g_1 G g_3 [g_{m4} + g_4]} \quad (3)$$

The parallel capacitance $C_p = C_1$ and the parallel resistance $R_p = 1/g_2$.

The resonance frequency ω_o is given as

$$\omega_o = \sqrt{\frac{g_{m1} g_{m2} g_{m3} g_{m4} + g_1 G g_3 [g_{m4} + g_4]}{G C_1 C_3}} \quad (4)$$

The quality factor Q_o at ω_o is given as

$$Q_o = \frac{\sqrt{\frac{g_{m1} g_{m2} g_{m3} g_{m4} + g_1 G g_3 [g_{m4} + g_4]}{G C_1 C_3}}}{\left[\frac{g_1}{C_1} + \frac{g_1 g_3 C_2}{G C_1 C_3} + \frac{g_3}{C_3} - \frac{\omega^2 C_2}{G}\right] g_4} \quad (5)$$

3. Design of LNA with input matching network using Active Inductor

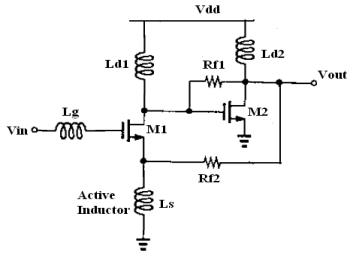


Fig 3: Circuit diagram of LNA with input matching network

The design of low noise amplifier comprises two stage amplifiers with resistive feedback as shown in Fig.3. The first stage of the amplifier is the common source configuration with source inductive degeneration and gate inductance. L_g ,L_s and c_{gs} of M1 forms input impedance matching network of the LNA. L_s is the source degenerative inductance which can be replaced by the tunable active inductor which is used to make the input impedance matched to the antenna impedance to prevent the incoming signal reflections between antenna and the LNA. The second stage of the amplifier is also the common source amplifier with resistive feedbacks to obtain low noise and high stable output. R_{f1} is voltage current feedback used to lower the transimpedance of the network and R_{f2} is the voltage-voltage feedback which is used to stabilize the output voltage amplitude in spite of load variations.

From the small signal analysis of the LNA, the input impedance is calculated using the equation (7) as given below,

$$Z_{inLNA} = j\left(\omega (L_s + L_g) - \frac{1}{\omega C_{gs}}\right) + \frac{g_m L_s}{C_{gs}} \quad (7)$$

The resonance frequency is given as,

$$\omega_o = \frac{1}{\sqrt{(L_s + L_g) C_{gs}}} \quad (8)$$

4. Simulation Results

4.1 Active Inductor

The simulations are carried out in 180nm CMOS process using HSPICE simulator. The transistor sizes (W/L in μm) are m1 (1.5/0.12), m2 (1.5/0.12), m3 (3/0.12) and m4 (3/0.12) of Fig. 2. The gate bias voltages are kept as Vb1=0.2V and Vb2=0.25V. The controllable current sources are I_1=90μA, I_2=80μA and I_3=100μA. The small signal parameters, gm_1 = 523μS, gm_2 = 724μS, gm_3 = 273μS, gm_4 = 873mS, g_1= 91μS, g_2= 84μS, g_3= 769μS, g_4= 109μS, C_1=1.87fF, C_2=1.53fF, C_3=4.03fF, C_4= 3.81fF and G= 1331μS are found from the operating points. Using these parameters in the equations (4) and (5) the resonance frequency and quality factor are calculated to be f_o=7.84GHz and Q_o=604 respectively.

To verify the designed equations, the circuit of Fig. 2 was simulated.

The simulated frequency response of Z_{in} is shown in Fig. 4. The magnitude of Z_{in} is nearly 150dB and the phase change is from +90◦ to -90◦. The magnitude response shows that it has real term and imaginary term. It is constant at 58dB up to 1.5 MHz which is equivalent to the real term. The real term is the series resistance R_s, which is calculated to be 154Ω. The response is increased from 1.5 MHz to 7.94 GHz which is equivalent to the imaginary term, the equivalent inductance L_{eq}. The value of inductance ranges from 125nH to 1530nH. Since it has less series resistance, the inductor loss is reduced. From the real and imaginary values of the simulation results, the quality factor Q_o is calculated to be 497 at the frequency f_o=7.94GHz. Fig. 5 shows the variation of Z_{in} for different values of controllable current source I_2. When I_2 is varied from 50μA to 120μA, the Z_{in} brings corresponding changes in R_s and L_{eq}. Therefore, the quality factor can be tuned through the controllable current source I_2. The center frequency f_o is tuned through the current source I_3 of Fig. 2 from 30μA to 100μA as shown in Fig 6. The proposed active inductor also features low power dissipation of 0.6mW and noise output voltage of 9nV/√Hz. Fig. 7 shows the simulated noise voltage of the active inductor.

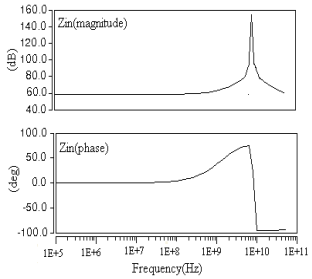


Fig. 4: Simulated Frequency Response of Input Impedance

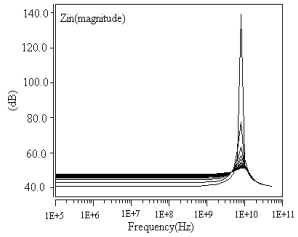


Fig. 5: Quality factor Tuning of the Active Inductor

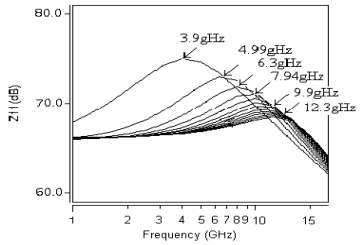


Fig. 6: Centre Frequency Tuning of the Active

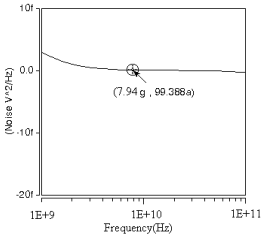


Fig. 7: Noise Voltage of the Active Inductor

The above simulation results show that the active inductor has better tuning of quality factor and center frequency. Table 1 compares the performance parameters of the active inductor with the literature of [7] and [8], shows that the designed active inductor has good quality factor, wide inductive bandwidth, low power consumption, very less noise and wide tuning capability.

Table 1: Comparison of the performance parameters of the active inductor

Parameter	**Ref. [7]**	**Ref. [8]**	**This work**
Technology	0.20μm/1.8V	0.13μm/ 1.2V	0.18μm/1.2V
Inductive BW	n.a	300MHz -.32GHz	1.5MHz-7.94GHz
L(nH)	29	38-144	125 – 1530
Q_L(max)	n.a	3900@5.7GHz	497@7.94GHz
P_{dis}(mW)	4.4	1	0.6
Noise	0.8μV/√Hz	69.31μV*	9nV/√Hz

4.2 Low Noise Amplifier

The simulation results of Low noise amplifier shows that it has the forward transfer gain S21 of 18dB as shown in Fig 8. and consumes power of 5.2mW. Fig 9: shows the designed LNA has low noise figure of 3dB for the frequency range 1GHz to 5GHz.

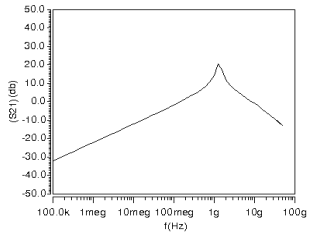


Fig. 8: Gain S21 of LNA

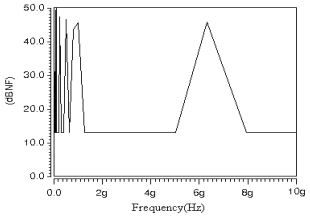


Fig. 9: Noise Figure of LNA

5. Conclusion

A Tunable CMOS active inductor and LNA are simulated in a180nm CMOS process. The simulation results of active inductor show that the circuit has wide inductive bandwidth, high resonance frequencies, low power and low noise which make it suitable for designing RF front end circuits. The designed active inductor is used in the input impedance matching network of LNA,thus it achieves high gain, low noise figure and consumes low power.

6. Acknowledgements

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7. References

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