

## Simulating Nanowire Defects

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**Abstract.** Nanowire based crossbars is considered one of the most promising technologies to implement the next generation digital systems due to its ability to implement and densely pack both logic and memory systems in a very small area using organizations such as crossbar. However, due to the bottom-up approach used in their manufacturing process, the occurrence of defects within nanoscale structures is inevitable which in turns demands a proper identification. In this paper we analyze the appropriateness of using stuck-at fault model when generating tests for various defects. Our simulation experiments show that tests generated using stuck-at models can effectively detect all defects within gates implemented using nanowires.

**Keywords:** Nanowire, Defects, Stuck-at Fault model, Simulation

### 1. Introduction

Nanometer crossbar based electronic systems are believed to be the next generation platform to implement various digital and memory systems due to their regular structure and capability to organize nanowires efficiently. A tremendous amount of research has been devoted to the implementation of the next generation electronics systems past the current technology node and into the sub-nanometer era [1, 2]. The current research trend revolves around the augmentation of conventional CMOS circuits with nanowires and carbon-nano tubes to realize different digital systems. This type of integration allows the designs to use the reliability of CMOS process in combination with the density characteristic of nanotechnology.

Current CMOS technology uses top-bottom manufacturing approach whereas nanotechnology based structures use stochastic self-assembled bottom-up approach where a high degree of defects is very likely to occur. Due to the increased probability of defects, post fabrication configuration is normally used to implement the required design after all defects have been identified and localized. Thus, defect-aware fault-tolerant logic mapping in nanotechnology crossbars is considered one of the highly active research areas nowadays [3, 4, 5].

Even though the test of nanowire based crossbars is rather an important topic, only limited number of researchers have discussed this issue [1, 6, 7, 8]. Most previous work discusses the test of crossbar pre-configuration where the purpose of the test is to locate defective logic blocks or interconnects. Moreover, in [6] the authors proposed modeling nanowire based logic gate defects as logical faults.

In this work, we simulate the behavior of defects in AND gates (when placed in a function of cascaded ANDs) implemented using nanowires and assess the appropriateness of using the stuck at model to generate tests to detect the various defects.

The remainder of the paper is organized as follows: section 2 gives an overview of crossbar nanoarchitecture and the implementation of AND gates using nanowires. Section 3 discusses defects as well as fault models of the a nanowired AND gate, and presents the test vectors used in the simulation. The test procedure for the various defects is discussed in section 4. Conclusion and future work is highlighted in section 5.

### 2. Crossbar Based Nanoarchitecture

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Crossbar architecture is the workhorse used in nanotechnology due to its density characteristics. Nanocrossbars are constructed from two perpendicular sets of Nanowires (NWs) and crosspoint junctions. NWs are made up of semiconducting materials such as silicon or germanium with typical diameter of 3 nm and length of up to hundreds of micrometers. When heavily doped, NWs exhibit metal-like conductivity characteristic whereas when lightly doped behave as semiconductor (p-type or n-type, depending on dopant). Unlike other nanoscale structures (e.g. nano-tubes), Nanowire dimension, chemical composition, and electrical properties can be controlled precisely during manufacturing. As a matter of fact, two types of active devices can be constructed using nanowires by controlling the doping profile of such wires. This can be illustrated by doping a part of a nanowire with a p-type dopant followed by an n-type dopant which results in the creation of a p-n junction diode in the same nanowire. On the other hand, a field effect transistor (FET) can be constructed using two crossed nanowires separated by an insulator (such as silicon dioxide). One of the wires contains a lightly doped region which will act as a channel for the FET whereas the perpendicular nanowire (placed over the lightly doped region) will act as the gate.

In a crossbar architecture, switchable contacts are normally used at the crosspoints to construct a configurable system. These contacts can be switched between high and low resistance states by applying a high voltage across them (i.e.  $\pm 2V$ ). Such crosspoint structures are normally used as the basic building blocks for nanoscale non volatile memory where high voltage is used to write data and low voltage is used for reading. Moreover, these programmable crosspoints allow the realization of programmable wired-planes and interconnects [1]. By programming multiple crosspoints to their ON states, a wired-OR is implemented by connecting a vertical (i.e. input) nanowire to a horizontal (i.e. output) one. If we restrict the connectivity of a single row (i.e. horizontal nanowire) to each column, then we can route any input signal to any output thus providing a programmable interconnect structure.

When implementing logic circuits, the output signal draws current directly from the input, therefore, output lines may not be driven to high voltage as their input counterparts. This necessitates the need for signal restoration which is normally done using buffer or inverter circuit [1].

### 3. Defects and Fault Models

Due to the stochastic approach used in the manufacturing of nanowire crossbar array, it is expected that a large number of defects will occur in such structures. For this reason, logic implementation in such architecture is done post fabrication to avoid the usage of defective resources. Fault tolerant logic mapping is one of the most highly researched area when it comes to crossbar based logic implementations [3, 4, 5]. Previous work such as [6, 7, 8] discussed the modeling and test of crossbar or Nanofabrics based defects. In [7, 8] the authors discussed methods to identify defective Nanoblocks/Nanoswitch by examining the connectivity of these blocks and label them as defect-free or defective. In [6], the authors discussed the modeling of defects in Nanowire based logic implementation and their logical behavior as well as developing a fault model to represent these faults. This paper analyzes whether it is sufficient to use traditional automatic test pattern generators (ATPG) to generate tests that would detect the various defects in a circuit implemented in nanowires.

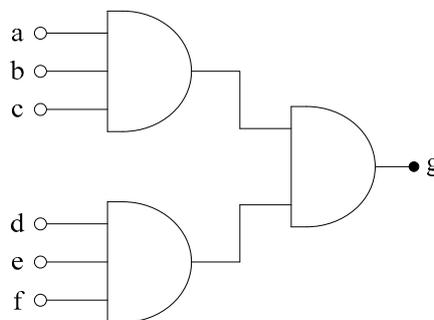


Fig. 1: Circuit Under Test (CUT)

When testing a digital circuit, ATPGs are normally used to generate the required test set to test the implemented circuit. Traditional ATPGs utilize stuck-at fault model to generate test set to detect the all

possible faults for the circuit under test (CUT). The stuck-at fault model assumes only a single fault can occur on interconnect lines of the CUT where such lines can either be stuck at logic level 1 or 0 (hence stuck-at 1/0). Moreover, the model assumes that faults within logic gates are not possible [9]. Even though the model is rather simplistic and seems unrealistic, it performs rather well when testing digital circuits implemented in CMOS technology. It was shown that it can detect multiple simultaneous faults as well as different fault types [9,10].

In order to generate tests, a fault list for all possible fault sites is generated and is used by the test generator to find the test set. In order to justify the appropriateness of the test set and its applicability to test nanowire defects, the detection capabilities of the tests must be analyzed. To perform such analysis, consider the circuit given in the Fig. 1. Using the stuck-at fault model, the fault list associated with this circuit consists of two faults (stuck-at 1 and stuck-at 0) for each line shown in the figure. A test set with 100% fault detection capabilities is shown in Table 1.

		Input					
		a	b	c	d	e	f
1	0	1	1	1	1	1	1
2	1	0	1	1	1	1	1
3	1	1	0	1	1	1	1
4	1	1	1	0	1	1	1
5	1	1	1	1	0	1	1
6	1	1	1	1	1	1	0
7	1	1	1	1	1	1	1

Table 1: CUT Test Set

When nanowires are used to implement any logic gate, the defects that can occur can be categorized as shorts or opens in the various elements which implement the basic gate [6]. For example, when an AND gate is implemented using nanowires, it looks as shown in Fig. 2. Therefore, when such structure is used, open/short can occur in the diodes, contact resistance, or between the inputs/output nodes. In the next section, we simulate the behavior of such defects and discuss the detection capabilities of the test set generated using stuck-at model.

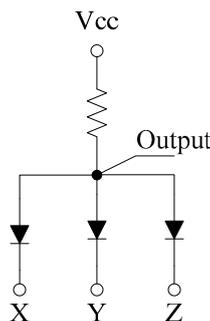


Fig. 2: AND Gate Implementation

## 4. Simulation Results

In order to study the effectiveness of test set generated by traditional ATPG, we simulated the behavior of the logic circuit shown in Fig 1 in the presence of defects. We compared the behavior of the fault-free and defective circuit and show whether the test set is capable of detecting these defects. Moreover, we describe the necessary conditions for each defect and correlate it to how the test set developed for stuck-at faults was able to detect the defect.

### 4.1. Experimental Setup

The circuit shown in Fig. 1 was implemented in Simulink MATLAB and the test set shown in Table 1 was simulated. Five different defective variation of the circuit were similarly implemented and simulated; each circuit contains a single defect in one of the AND gates. Four of the simulated AND defects are shown in Fig. 4 (only input-to-output short is not shown).

## 4.2. Experimental results

Due to space limitation, only the resulting output of the fault-free circuit in comparison to a circuit with the defect shown in Fig. 3a is presented in Fig. 4. Comparing both wave forms, it can be seen that the test vector 2 and 3 detect this defect since the output waveform for both circuits are not identical. The necessary condition to excite this fault is to have a high voltage on the input of the shorted diode while having at least one of the other diode inputs grounded. In defect-free circuit, such bias condition will forward bias the diode with low voltage resulting in current flow. The output voltage will be equal to the voltage across the diode which will be very low thus resulting in a logic 0 output. However, in the defective gate (Fig. 3a), the output voltage is equal to the shorted diode input (X in this case) regardless of the other inputs (i.e. Y and Z); thus outputting a high voltage level (logic 1).

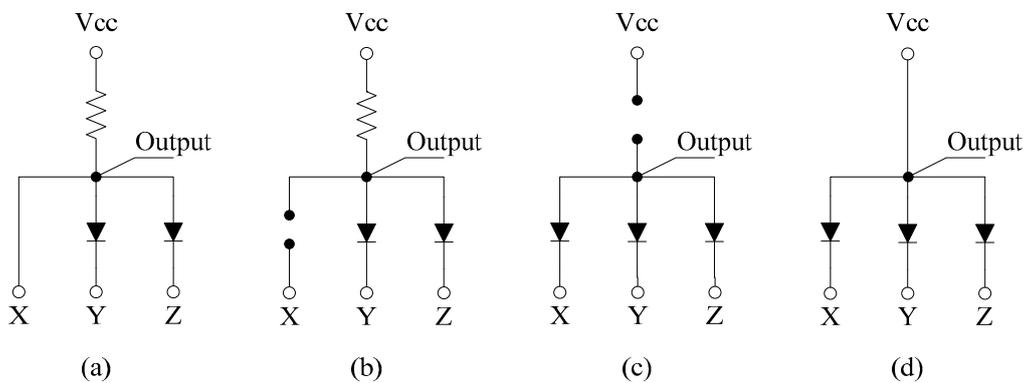


Fig. 3: Simulated Defects

As for open diode defect (Fig. 3b), applying low voltage on defective diode while having all other diodes inputs high will result in high output whereas the defect-free one will have low output voltage. This is due to the fact that the open diode will not allow current to flow (similar to the remaining ones which are reverse biased in this case) thus rendering the output to a high voltage.

When there is a defect in the crosspoint between nanowires, such defects will result in an open/short in the AND gate pull-up resistance as shown in Fig 3. If this resistance is shorted the voltage at the output node will always be high. However, if the resistance is opened, the voltage at the output will equal the highest voltage at the gate input. The case is detected by any test vector that has one input with low voltage (i.e. test vector 1, 2, or 3 for a defect in the top AND gate).

The last defect that was simulated was a short defect between input and output lines of the AND gate. Such defect will result in an output voltage which follows the voltage of the shorted input regardless of the state of the other the inputs. Thus a test for this defect should have a high voltage at the shorted input while at least one of the other inputs is grounded (i.e. test vectors 1-3 in Table 1)

From the simulation results, we able to detect all internal defects (the ones presented in Fig. 3 as well as an output-to-input short) of the top AND gate in Fig. 1 using test set {1, 2, 3} whereas test set {4,5,6} was able to detect those in the bottom one. Thus, the two groups of test sets were able to discover all the defects in the second level AND gate.

The previous discussion concludes that traditional ATPGs are effective in generating test sets that will detect all defects in nanowire realizations of a function implementation using AND gates.

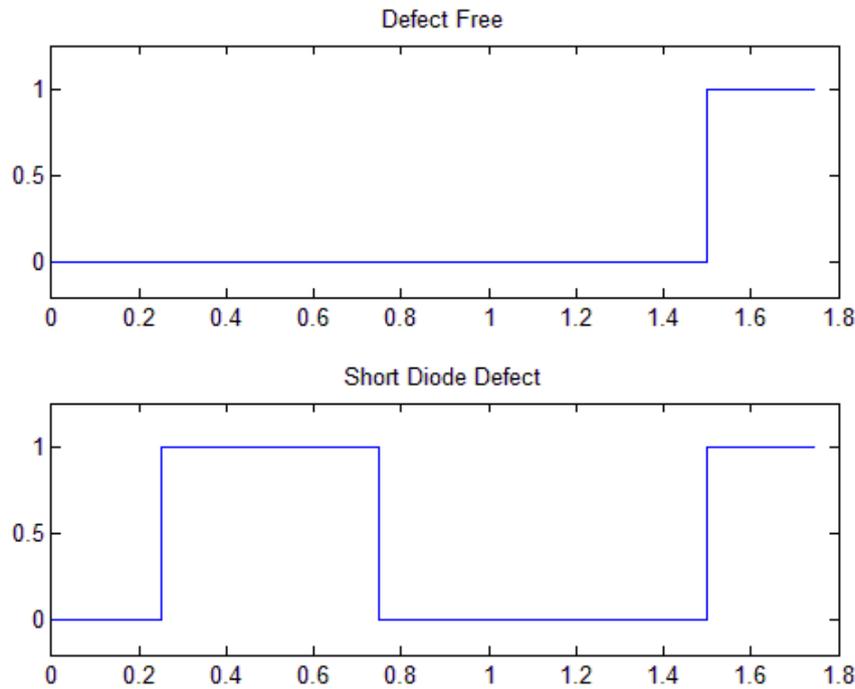


Fig. 4: Simulation Results

## 5. Conclusion

In this paper, we analyzed nanowire based AND-gate defects and simulated their behaviors using a test set generated by a traditional ATPG engine. Simulation results shown that the test set generated is capable of discovering all defects modeled in this work. Such findings confirm the applicability of using stuck-at fault model when generating tests for nanowire based realization of a function implementation using AND gates. Future work should investigate the applicability of the stuck-at model to other types of gates/functions that are implemented using nanowires.

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