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Non-ideality Analysis of Folding-Interpolating ADC

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Abstract. This paper introduces a new non-ideality model focusing on folding and interpolating analog to digital converter (FIADC). Some non-idealities are studied and analyzed in the proposed model including reference voltage varies which are caused by the resistance errors, output voltage offset of the track-hold array with different input voltages and the trade-off between gain and linearity of folders. The model is simulated based on an 8 bit FIADC and simulation results show the evaluation of the FIADC performances which can also be used for circuit design.

Keywords: Folding and interpolating, track and hold, folder, behavioral modeling

1. Introduction

Among the kinds of analog to digital convertors (ADC), folding and interpolating ADC (FIADC) is an efficient architecture for middle precision and high speed ADC design [1]. In older to make a good trade-off between speed and precision as well as achieve short design cycle, a non-ideal model of FIADC is presented in this paper. Based on non-ideal analysis of each building block, performances of FIADC are simulated in the model. At last, the simulation results are summarized to guide the circuit design.

2. Non-ideal Factor Analysis

FIADC achieves high speed as coarse channel and fine one convert signals at the same time [2]. There are some non-ideal factors in modules which are analysed as follows.

2.1. Resistor Ladder

The signal feed-through model presented by Venes is always used in the past resistor ladder analysis, which focuses on the reference voltage jitter coupled from input signal through gate capacitor of input transistor. However, it can be avoided efficiently in a fully differential architecture. Mismatches and resistors manufacturing accuracy will affect the reference voltage.

2.2. T/H Array

- 2.2.1 Output Common-mode Voltage Offset

In T/H array, different input reference voltages of each T/H cell cause different output common-mode voltages. Although the difference doesn't affect the correct zero-crossing of T/H array, it causes each differential pair of folder working in different DC situation, which introduces zero-crossing error of folder. Take single common-source amplifier in Fig.1 for example.

In Fig.1, M1 is the amplify transistor, M2 is the current source, and R_{load} is the load resistor. Therefore, the circuit can be analyzed with following equations.

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$$V_{out} = V_{dd} - R_{load} * \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{s1} - V_{th1}) \rightarrow V_{out} \propto a(V_{in} - b)^2 \tag{1}$$

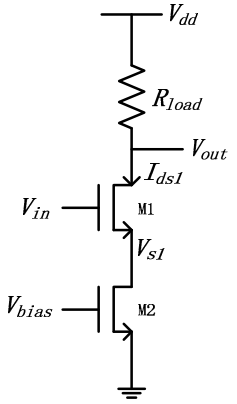

Fig.1Common-source amplifier

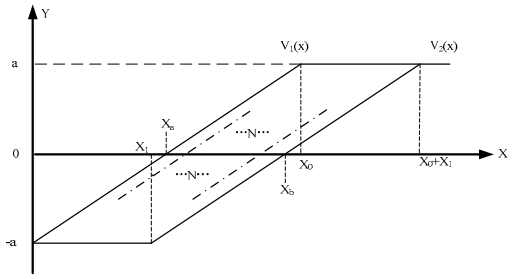

Fig.2 Transfer function curve of folder and interpolating signals

In which, *a* and *b* refer to eccentricity and local minimum of output common-mode voltage bias parabolic curve. It shows that the different output voltages of cells in T/H array are approximately in direct proportion to square of input voltages.

- 2.2.2 Gain Error

In T/H array, each T/H cell has different gain because of different input reference voltages. Take the circuit in Fig.1 for example.

$$Av = -\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{s1} - V_{th1}) \cdot R_{load} \rightarrow Av \propto -cV_{in} \tag{2}$$

In which, *c* is linear parameter. It shows that absolute value of gain of each T/H cell is approximately in direct proportion to the input signal amplitude.

Meanwhile, the switched-capacitor or other similar circuit will introduce clock jitter, clock offset and settling time and other non-ideal factors.

2.3. Folder

In older to achieve a correct interpolating function, at least a half linear range of folding transfer function curves should be covered by adjacent one. In Fig.2, two solid lines V1 (x) and V2 (x) are output of adjacent folders. Their equations are shown as Eq.3. Dashed lines show the interpolating signals generated by V1 (x) and V2 (x) with the interpolating rate of *N*. The expression of the interpolating signal I_i(x) is showed in Eq.4.

$$V_1(x) = \begin{cases} \frac{2a}{X_0} \cdot x - a & x \le X_0 \\ a & x > X_0 \end{cases} \qquad V_2(x) = \begin{cases} -a & 0 \le x \le X_1 \\ \frac{2a}{X_0} \cdot x - \left(1 + \frac{2X_1}{X_0}\right) \cdot a & X_1 < x \le X_0 + X_1 \\ a & x \le X_1 \end{cases} \tag{3}$$

$$\begin{aligned} I_i(x) &= \frac{(N-i)}{N} V_1(x) + \frac{i}{N} V_2(x) \\ &= \begin{cases} \frac{N-i}{N} \cdot \frac{2a}{X_0} \cdot x - a & x \le X_1 \\ \frac{2a}{X_0} x - \left(\frac{i}{N} \cdot \frac{2X_1}{X_0} + 1\right) a & X_1 < x \le X_0 \\ \frac{2ia}{NX_0} x - \frac{i}{N} \cdot \left(1 + \frac{2X_1}{X_0}\right) a + \frac{(N-i)a}{N} & X_0 < x \le X_0 + X_1 \\ a & X_0 + X_1 < x \end{cases} \end{aligned} \tag{4}$$

The Eq.4 shows that only when $X_1 < x < X_0$, the slope of each interpolating signal is the same. Moreover, according to equations of V1 (x) and V2 (x), zero-crossing position of the folding signal can be achieved as well as that of interpolating signals. Then Eq.5 can be derived.

$$X_1 \le \frac{X_0}{2} + \frac{i}{N} X_1 \le X_0 \quad \underline{N \ge 2} \quad \frac{N-1}{N} X_1 \le \frac{X_0}{2} \tag{5}$$

It can be seen that X_1 needs to be twice as X_0 when N is infinitely large, therefore, at least a half the linear range of the input-output curve of the adjacent folders output should be covered. In circuit design, the circuit gain and linear range will affect this coverage.

3. Modeling Method

Classic 8bit FIADC architecture is modeled based on Matlab which is shown in Fig.3. In this system, the coarse channel converts three bits, while the fine one converts five bits. Meanwhile in the fine channel, there are four folders with folding rate of eight and the interpolating rate of eight as well.

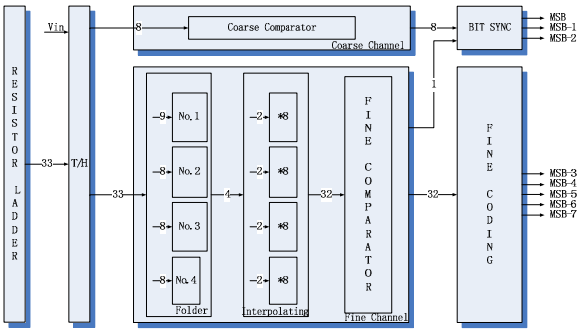

Fig. 3 8bit FIADC architecture

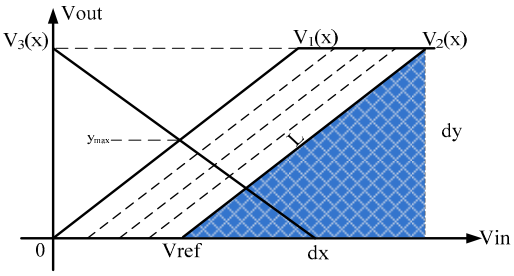

Fig. 4 Output versus linear range and gain

3.1. Resistor Ladder

Non-idealities of resistor ladders analysed above can be equaled to resistance changes. Therefore, assume that there is random Gauss jitter in a resistor in ladder, whose mean is zero, and the variance is ΔR. Then the output reference voltages can be expressed below:

$$vref(i) = \frac{iR + \sum_{j=1}^{i} \Delta R(j)}{AR + \sum_{j=1}^{j=A} \Delta R(j)} \tag{6}$$

vref(i) refers to the i-th reference voltage value, A represents the total number of resistor, ΔR refers to the resistance offset caused by manufacturing variations or feed-through from T/H array.

3.2. Folder

In folder modeling a saturation block is applied which defines the maximum output voltage. The relationship between the output versus linear range and gain is indicated in Fig.4. According to the triangle relationship between the output versus linear range and gain, $dy_{L,K}$ in Eq.7 can be derived. Meanwhile, it can be seen that maximum output $dy_{LSB,K}$ will be achieved by the interception of V3 (x) and V1 (x). That is to say the scan of output which is larger than $dy_{LSB,K}$ is meaningless. Then the output can be achieved as Eq.8.

$$dy_{L,K} = \frac{LK}{2\sqrt{K^2+1}} \qquad dy_{LSB,K} = \frac{1}{16} LSB \cdot K \tag{7}$$

$$dy = Min(dy_{L,K}, dy_{LSB,K}) \tag{8}$$

In which, the blue triangle hypotenuse is the output linear range L, and the ratio of the two cathetuses is the gain K.

Other modules are modeled according to the analysis above.

4. Results and Analysis

Ideal FIADC Model has a SNR of 49.95dB when the sampling frequency is 800MHz and the input signal frequency is 383.1MHz. Non-idealities are simulated based on this model with the same input signal and sampling signal frequency.

Fig.5 shows the mean of 100 simulation results of the system performance caused by the resistor ladder reference voltage jitter. It shows that the jitter obviously impacts on the odd harmonics, particularly third harmonic and further affects the SINAD.

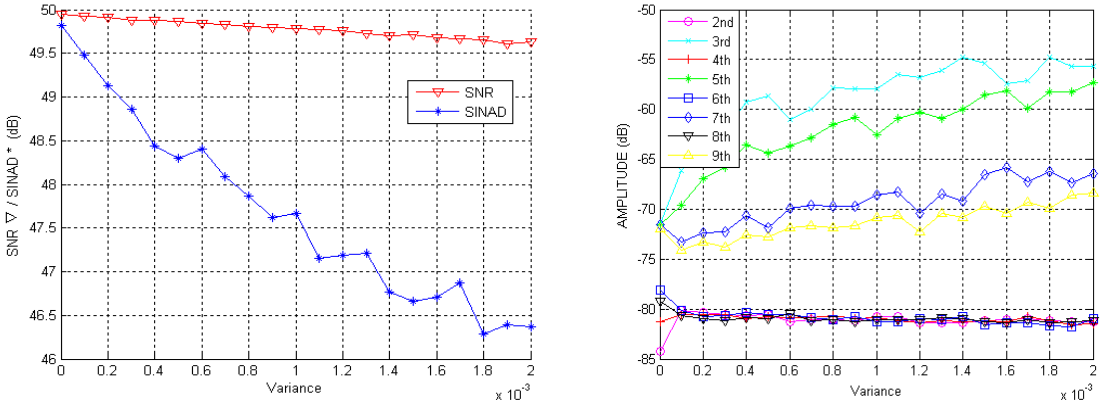

Fig. 5 SNR, SINAD and harmonic distortions versus resistor jitter

Fig.6 is the system performances affected by T/H array output common-mode offset. It shows that the impacts of odd and even harmonics are very obvious, which decreases the SNR and SINAD significantly as offset increases.

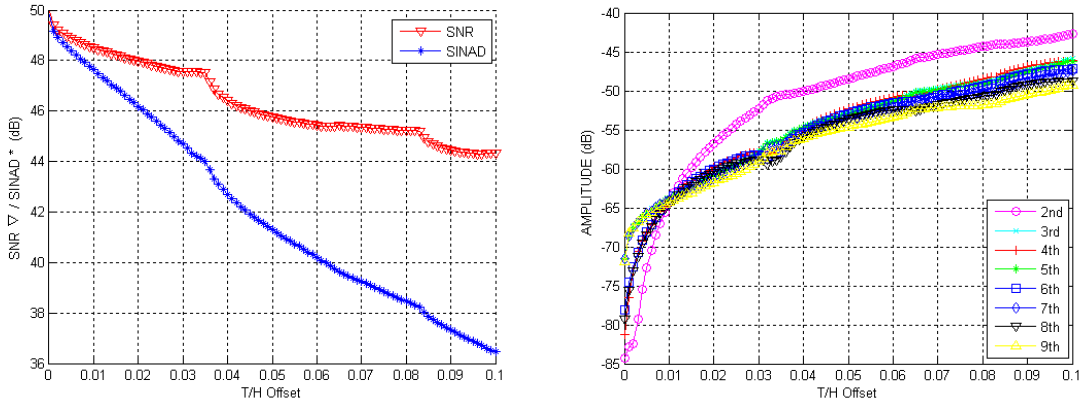

Fig. 6 SNR, SINAD and harmonic distortions versus T/H output bias

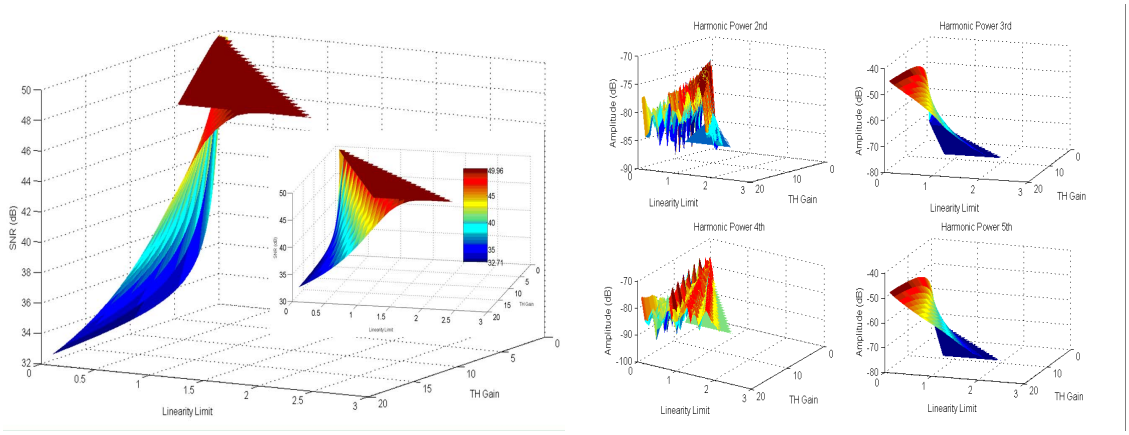

Fig. 7 SNR and harmonic distortions versus linear range and gain

The following Fig.7 shows the surface plot of the system performance affected by the gain and linear range of folders. The red flat triangle areas in figures are the appropriate combination of gain and linear range. As analyzed in Eq.8, the scan of saturation output which is larger than the one decided by gain and least significant bit is meaningless. It also can be seen that the SNR decreases when the odd harmonics increase beyond the red flat triangle area.

For a larger than 7.5 bit ENOB, the simulation results are summarized in the following table, which can be used to guide the circuit design.

Tab.1 Modeling simulation results

Performance	System SNR	Resistance jitter variances	T/H array output offset	Folder gain	Folder Linear range
Requirement	>48dB	<0.7	<0.06*Vref	12±2dB	(0.8±0.2)*Vref

5. Conclusion

The aim of the paper is to introduce the non-ideality FIADC model. According to the theoretical analysis of some non-idealities of system, the model is simulated based on an 8 bits folding and interpolating ADC. Simulation results show that reference voltage bias caused by resistor ladder jitter increases the odd harmonic distortions. SNR and SINAD also drop while output common-mode voltages differences of T/H array caused by different input voltages increases. In the surface plot of output saturation decided by linear range and gain of folders, the proper gain and linear range combinations exit in a certain triangle area, SNR and SINAD decline quickly outside this area. These results can also be used to specify the requirements in circuit design.

6. Acknowledgement

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7. References

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