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Design of 3.5 GHz Low Supply Receiver Front-Ends for WiMAX Application

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Abstract. The objective of this project was to enable a receiver at a bias voltage at 0.6 V. This design employed a low-noise amplifier (LNA) with a cascade structure and a mixer adopting the transformer isolation method for a separately biasing transistor. It has the equivalent effect of using a Bias Tee for the same separate biasing purpose, and occupies an area only the size of a transformer, which greatly decreases the area used on the chip. This design not only drives the mixer at 0.6 V, but also reduces the manufacturing cost of the chip.

This design adopted the 0.18 μm TSMC RF CMOS processing technology. Through measurement, the direct current for 0.6 V bias was 19 mA, and the receiver gain could reach up to 20 dB. Reflection coefficients were all below -10 dB; noise figure was 3.9 d; the whole area was 1.27 mm by 1.07 mm.

Keywords: Low supply, receiver, transformer

1. Introduction

The main goals of IC design for this project are as follows: (1) To obtain a low-cost and highly-integrated CMOS process technology; (2) To integrate single or multiple systems to the system on chip (SOC) of a single chip; and (3) To reduce the overall power consumption of the circuit.

Therefore, a low-cost and highly-integrated CMOS processing technology is a good choice for IC modularization. Because the receiver is used in motion, operating at low-voltage and with low power consumption are critical indicators in receiver design. This design has an operating voltage at 0.6 V, and can overcome issues attributed to low-voltage operations. The circuits integrated on the chip include: (1) a low-noise amplifier (LNA); (2) a passive balun; and (3) a low-bias frequency mixer.

2. Contents

Fig. 1 is the schematic view of the integrated receiver front-end of this project. A cascade LNA is the first-stage input, which improves overall receiver sensitivity with its features of high-gain and low-noise. Then the radio frequency (RF) signal received is converted to an intermediate frequency (IF) through a down-conversion mixer, and output with a differential signal.

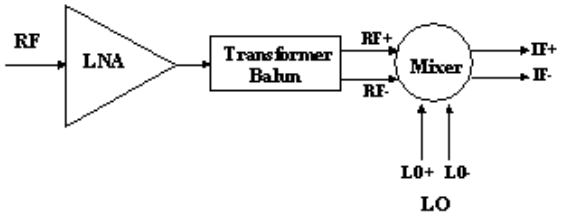


Fig. 1 Schematic View of the Entire Circuit

2.1. Low-Noise Amplifier (LNA)

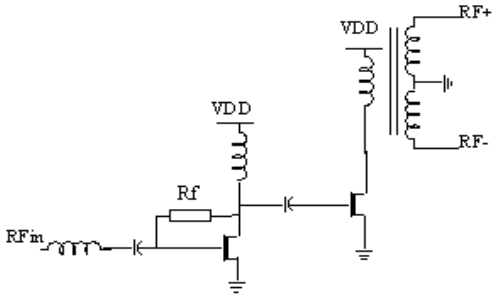
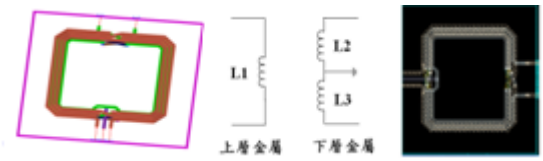


Fig. 2 Schematic View of the LNA Circuit

Fig. 2 is the schematic view of the LNA circuit. Because the bias voltage of the cascade circuit must operate above 1 V, all LNAs in this design adopt a cascade structure, such that the transistors of each stage may be biased at 0.6 V. Since the next stage mixer has a differential structure, a transformer balun is used for output loading, and two different mutually-inducted inductors become the transformer. L1 is the loading of LNA, and the center of the second turn of the inductor connects to the ground to attain the function of single-ended differential conversion. A formula is used to calculate the inductance ratio of the impedance matching between the two stages, and the properly designed inductance ratio completes the inter-stage matching. With this method, an overlapping inductor may complete the matching and signal conversion, thus reducing the large area for matching circuits.



Upper-Level Metal Lower-Level Metal

Fig. 3 Transformer Balun

2.2. Low-Bias Voltage Mixer Design

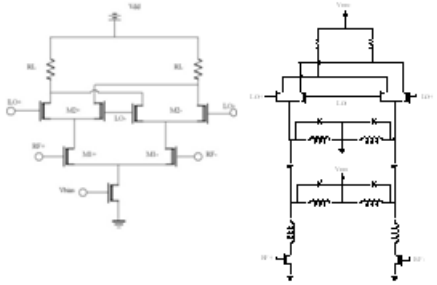


Fig. 4 (a) Gilbert Cell Mixer; (b) Low-Bias Voltage Mixer [13]

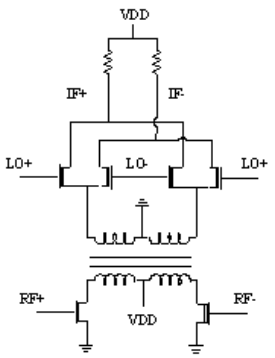


Fig. 5 Mixer Structure

Because the mixer includes a transduction level and a switch level, its bias voltage cannot be too low. This design employs the conventional Gilbert cell mixer, and separately biases the transistor with a Bias Tee

as suggested in [13], so as to drive the entire mixer at 0.6 V. However, the area of the chip may become too large because of the large quantity of inductors and capacitors used; thus, this design adopts a transformer for separating two ends of the transistor of the Gilbert cell mixer, which separately biases the transistor at the two ends for direct current. The effect for a small signal is the same as that when using the conventional Gilbert cell mixer. This method successfully enables each transistor in the mixer at 0.6 V, reduces the power consumption required for the mixer by separate biasing, and shrinks the area used on the chip.

3. Simulation and Measurement Results

This design used Agilent ADS for the overall low-voltage receiver, simulated with the 0.18 μm TSMC 1P6M CMOS standard process, and added a PAD equivalent circuit to simulate the parasitic effect. The entire circuit operated at 0.6 V, and total power consumption was 11 mW. Fig. 6 to 11 are comparative diagrams for simulations and measurements. Fig. 6 represents the input-end reflection coefficient. The simulations and measurements were all below -10 dB at 3.5 GHz. Fig. 7 indicates the output-end reflection coefficient (S33); the simulations and measurements were below -10 dB at 300 MHz. According to Fig. 8, the simulations and measurements were below -31 dBm at P1dB, and part of the simulations and measurements of the conversion gain were at 20 dB. As for the double-side band noise figure (NF-dsb), shown in Fig. 9, the simulated value was 3.4 dB, and the measured value was 3.9 dB. Fig. 10 represents the IIP3. Fig. 11 is the schematic view of the chip, with an area of 1.27 by 1.07 mm2. Table 1 is a chart comparing simulations with measurements.

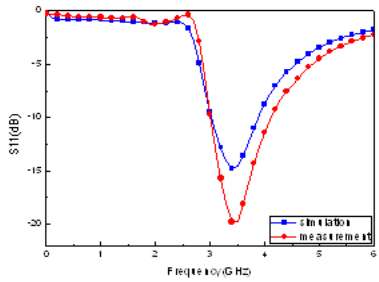


Fig. 6 Comparative Simulations and Measurements (S11)

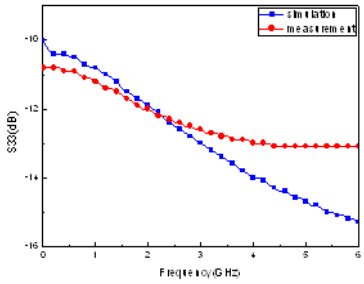


Fig. 7 Comparative Simulations and Measurements (S33)

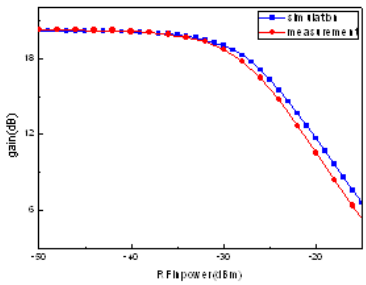


Fig. 8 Comparative Simulations and Measurements (P1dB)

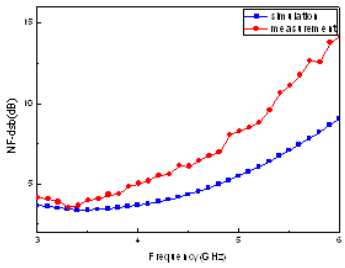


Fig. 9 Comparative Simulations and Measurements (DSB)

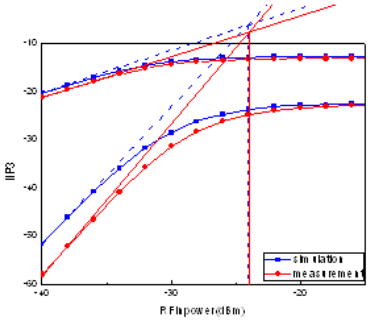


Fig. 10 Comparative Simulations and Measurements (IIP3)

Table 1. Comparative Chart for Simulations and Measurements Results

Development of the 3.5 GHz WiMAX Low-Voltage Receiver		
Parameters	**Simulation**	**Measurement**
RF Frequency (GHz)	3.5 GHz	3.5 GHz
IF Frequency (MHz)	300 MHz	300 MHz
Supply Voltage	0.6 V	0.6 V
Conversion Gain (dB)	20.1	20.2
S11 (dB)	<-10	<-10
S33 (dB)	<-10	<-10
NF-dsb (dB)	3.4	3.9
P1dB (dBm)	-31	-31
IP3 (dBm)	-24	-24
Power Dissipation (mW)	11	11

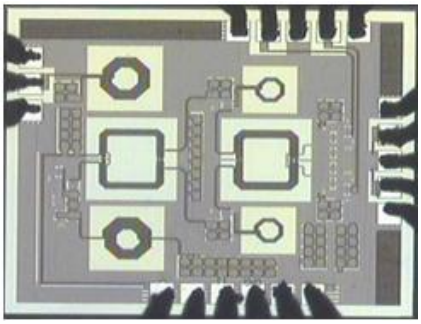


Fig. 11 Top View of the Chip

4. Conclusion

This is the design for a 0.6 V low-bias voltage WiMAX receiver developed with the transformer isolation technique, using a low-bias method in circuit design to reduce power consumption. After actual tapeout, based on the measurement results, it is found that the entire circuit may be driven at 0.6 V, and can reach up to a gain of 20 dB and a noise figure of 3.9 dB with a consumption of 11 mW. These features are similar to those which resulted from the simulation.

5. Acknowledgements

We would like to thank to the National Chip Implementation Center (CIC) for providing 0.18 μm TSMC CMOS processing technology for the completion of this circuit design. We also want to thank to the National Nano Device Laboratories (NDL) for its outstanding measurement environment and services.

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