A 3.1 - 10.6 GHz CMOS Low-Voltage Mixer with Active Balun Designed for UWB Systems

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Abstract. This paper presents the design of a 3.1-10.6 GHz down-conversion mixer for ultra-wideband (UWB) system with 0.18 μm SMIC CMOS technology. The mixer with an active balun was fabricated in the 0.18 μm IP6M standard CMOS process. The broadband mixer with an active balun achieve a conversion gain of 16 ± 0.1 dB and 7.6 – 11.8 dB on a double-sideband (DSB) noise figure. It also achieved an input third-order intercept point (IIP3) of -1.89 to -1.8 dBm. The mixer with active balun consumed 17.3 mW from a 1.2 V supply. This circuit did not match S11,or S33 to save chip area.

Keywords: mixers ;ultra-wideband (UWB)

1. Introduction

A direct down-conversion mixer is crucial to translate an RF signal to baseband signal. It dominates the UWB system performance on linearity, noise figure (NF), and conversion gain. Direct conversion structure is used mainly to cancel the image frequency. The mixer is located after the low noise amplifier (LNA), and directly manages the RF signal amplified by LNA. The performances of the mixer have a direct influence on the performance of the whole system. Therefore, the research of ultra-wideband down-conversion mixers has received considerable attention. In 2002, the FCC made 3.1 - 10.6 GHz available for UWB applications, and limited the output power of Tx to 41.3 dBm/MHz. This indicated that UWB system designs focused on providing low power, low cost, and wideband performance over a short distance. The design of UWB system elements differed from traditional narrow band applications considerably,and offered unique challenges.

2. Circuit Topology and Analysis

2.1. The main schematic of the mixer

The folded-switching mixer in this study operates at low supply voltages [9]. The goal was to reduce the voltage drops across the load resistors and the switching transistors. This study used a folded-switching mixer to achieve this goal because the typical Gilbert cell mixer has a larger voltage across the circuit than the folded-switching mixer. Fig.1 shows the folded-switching mixer.
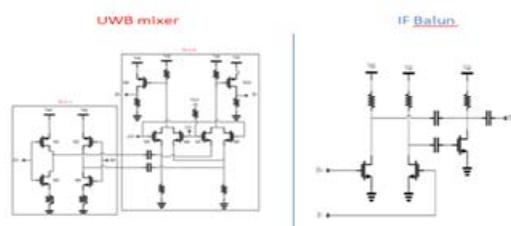

Fig. 1: The main schematic of the Circuit.

2.2. Block A

V_{odn} is the overdrive voltage of the NMOS transistor (M3, M4), and V_{odp} is the overdrive voltage of the PMOS transistor (M1, M2). V_{th} is the threshold voltage of the transistor. Therefore, the minimal supply voltage (Vdd_{min}) can be calculated by

$$Vdd_{min} = V_{odn,min} + V_{odp,min} + 2V_{th}$$

Assuming that the local oscillator signal is the ideal squarewave, g_mn is the transconductance of the NMOS transistors M3 and M4, andg_mp is the transconductance of PMOS transistor M1 and M2, RL is the load resistor, and ´Yn and ´Yp is the channel coefficient of NMOS and PMOS, respectively. The voltage gain and noise figure of mixer can be expressed as

$$G = \frac{2}{\pi}(g_{mn} + g_{mp})R_L$$

$$NF = 10\log\left(2 + \frac{4\left(\gamma_n g_{mn} + \gamma_p g_{mp}\right)}{R_s\left(g_{mn}+g_{mp}\right)^2} + \frac{\pi^2}{2\left(g_{mn}+g_{mp}\right)^2 R_L R_s}\right)$$

Block B

Block B consists of the switching stage and the IF buffer. The RF signal is delivered through the capacitor. The capacitor is also the dc block from the transconductance stage to the switching stage.

2.3. Active Balun

The IF ports are the differential ports; the addition of the active balun allows differential ports to combine one output port. They can provide some gain to increase total gain. Fig.2 shows the active balun.
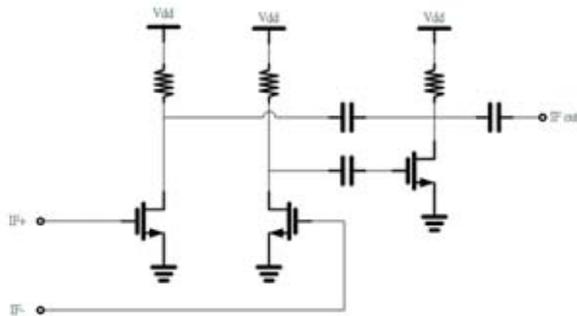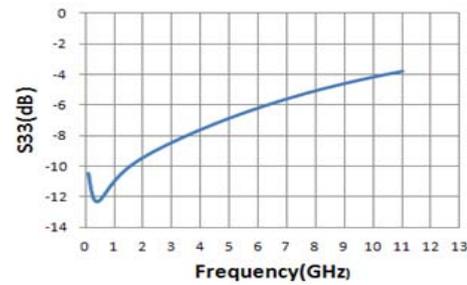

Fig. 2: IF balun.

Fig. 3: Simulated reflection coefficients (S33).

3. SIMULATED RESULTES

Advanced Design System (ADS) using 0.18 μm CMOS process TSMC model parameters was used to simulated the proposed UWB mixer with active balun. The UWB mixer with active balun operated with 1.2 V power supply and consumed 17.3 mW. Fig.4 shows the conversion gain (CG) of the mixer with active balun. This circuit achieved a 16 ± 0.1 dB conversion gain within the bandwidth. Fig.6 shows that the double-sideband (DSB) noise figure of this circuit is 7.6 – 11.8 dB. Fig.5 shows the input third-order intercept point (IIP3) of -1.89 to -1.8 dBm. Fig.3 shows the simulated reflection coefficients (S33).

Table 1 is a summary of implemented 3.1 - 10.6 GHz CMOS mixer. As shown in Table 1, our CMOS mixer exhibited the lowest power consumption; the simulation results demonstrated that the proposed mixer design methodology is suitable for 3.1 - 10.6 GHz UWB or even higher frequencies, such as wideband communication applications.
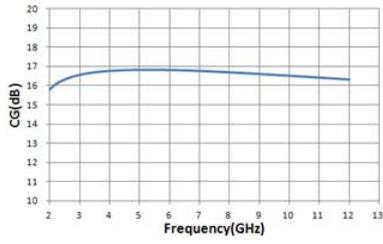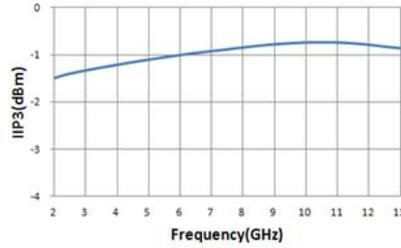
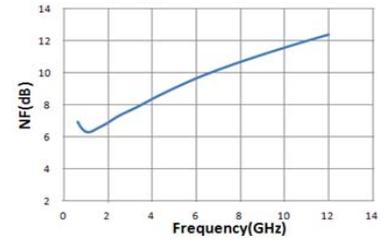Fig. 4: Simulated CG (dB). Fig. 5: Input third-order intercept point (IIP3). Fig. 6: noise figure (DSB).

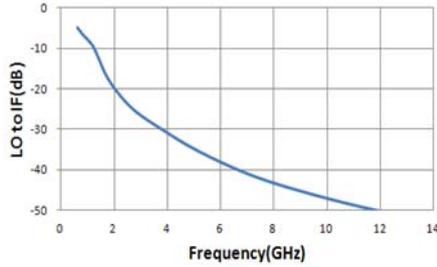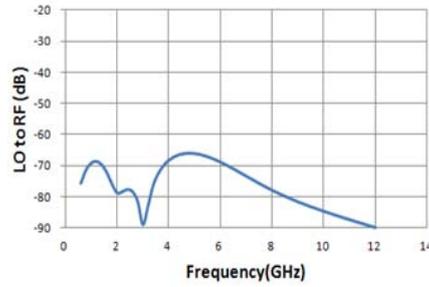Fig. 7: Simulated LO to IF. Fig. 8: Simulated LO to RF.

Table 1. Performance Summary And Comparison To Other Wideband 0.18μm Cmos Mixers.

	Frequency (GHz)	Mixer Type	Conversion Gain(dB)	Voltage Supply(V)	Power (nw)	Chip size (mm*mm)
This work	3.1-10.6	Folded-switching mixer+ Active balun	21 0.6	1.2	18	0.67*0.85
[1]	dc-30.5	Gilbert-cell	>5.9	4.9	9.8	0.45*0.45
[2]	3-8.7	Distributed mixer	3	1.8	10.8	1.4*1.1
[3]	0.3-25	Gilbert-cell+ Buffer	11	5	157	1*0.8
[4]	9-50	Gilbert-cell+ Buffer	>5	3.3	97	0.5*0.5

4. Conclusion

This paper presents a discussion of UWB applications, and focuses on low supply voltage, and high and flat conversion gain (16 ± 0.1 dB). Table 1 summarizes previously published wideband mixers. This study used a folded-switching mixer with low supply voltage, combined with an active balun.
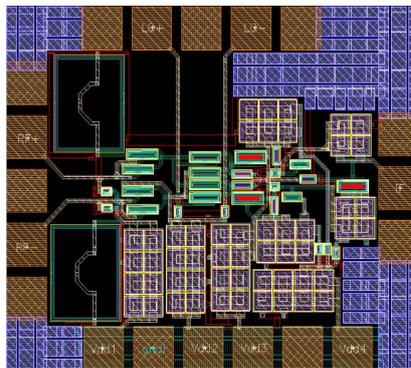
5. Acknowledgements

Fig. 9:Layout..

6. References

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