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Design and Implementation of Narrow-Band Linear Approximated Direct Digital Frequency Synthesizer

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Abstract. This paper presents a new approach to the design of narrow-band direct digital frequency synthesizer (DDFS) based on linear interpolation .In this search the segment slope's computation was included in the hardware, thus the ROM for storing those values is eliminated. The slope can be derived at the first sample of each segment as long as the Frequency Tuning word (FTW) is less or equal the segment's word length. ROM reduction has resulted in significant logic element (LE) saving and simplified the whole DDFS structure. The proposed DDFS has been simulated and tested over interested frequency range. The spurious free dynamic range (SFDR) of synthesized sinusoid achieved was 96 dBc. The proposed DDFS is more suitable for a variety important application under the signal analysis category including industrial and biomedical applications.

Keywords: Direct digital frequency synthesizer (DDFS); Phase to sine amplitude conversion; ROM-less DDFS.

1. Introduction (Use "Header 1" Style)

Direct Digital Frequency Synthesizer is an essential part in wireless communication systems. It has been applied to variety of areas such as frequency hopping spread spectrum (FHSS) system, wireless sensor network (WSN), digital cellular phone, and numerous other fields.

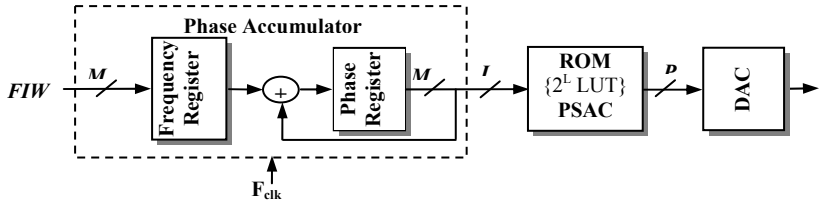

Fig. 1 The conventional structure of a DDFS

DDFS has one of the most important feature in which frequency, phase and amplitude modulation can be directly implemented. The conventional DDFS structure was first introduced by the Tierney et al. in 1971 [1].A block diagram of this architecture is shown in Fig. 1.It mainly has four basic blocks: phase accumulator, phase-to-sinusoid amplitude converter (PSAC), digital to analogue converter and low pass filter.

At each clock period, the phase accumulator adds an *M*-bit Frequency Tuning Word (FTW) to generate these phase values. After a certain number of clock cycles equal to $2^M/FTW$, the DDFS generates one complete synthesized sine wave cycle .Hence the output frequency is given by

$$f_{out} = \frac{FTW}{2^M} f_{clk} \tag{1}$$

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Most DDFSs use a wide phase accumulator to satisfy the frequency resolution requirements. However, this leads to a huge ROM with $2^L \times P$ sinusoid samples.The large ROM consumes high power and large area which is degrading the performance of DDFS. However, excessive power consumption must be alleviated in portable battery-powered disposable equipment, and this makes it necessary to use some compression techniques to reduce the ROM size while still retaining high spectral purity.

To reach such goals, several techniques have been proposed. These techniques include exploitation of trigonometric identities and approximation of the sine function. The alternative approaches were completely discarding the need of ROM by computing the samples of sine amplitude from the digital phase contents. The ROM elimination has been investigated in many researches, such as [2]-[6].

Piecewise linear approximation is an attractive method to generate a sine wave with a simple hardware realization. Implementation of the first order interpolation requires two ROMs. The first is used to store the values of slope and the other for the storage of initial values. The existing technique, based on piecewise linear polynomials was first introduced by Freeman [7]. He approximated the first quadrant of the sine function by 16 piecewise linear segments. Initial amplitudes and segment slopes were stored in two ROMs, the architecture also incorporated with multipliers, adders and an additional small ROM to store the correction values. In [8], the first quadrant of the sine function was approximated with linear segments of unequal lengths.

Langlois and Al-Khalili [9] introduced a multiplierless DDFS architecture. The multiplier was eliminated by properly selecting the segment slopes such that they can be represented with a limited number of signed digits. This architecture has replaced the multiplier and the ROM of the slope coefficients efficiently. But for high spectral purity demand, the circuit's complexity grew dramatically.

In this article we include the segment slope's evaluation in the hardware, thereby eliminating the need for the additional ROM.

2. The proposed design

Besides the sine symmetry property, the linear approximation method has been used to approximate the first quadrant of sine function by s straight lines; each line is defined by two coefficients, m_i and c_i. The i^{th} linear segment slopes coefficient m_i, can be calculated from the segment initial amplitude coefficients c_i as follows.

$$m_i = \frac{(c_i - c_{i-1})}{w}, 1 \le i \le s \tag{2}$$

Where $c_i = \sin iw$, and $w = \pi/2s$, the length of segment. Equation (2) can be realized by subtracting the c_i coefficients at first phase sample of each segments interval and then dividing the result by w. Periodically the ROM data bus holds an i^{th} segment initial amplitude coefficient for a certain clock cycle equal to

$$Clock\,cyclepersegment = \frac{2^{M-2-\log_2 s}}{FTW} \tag{3}$$

Where the $2^{M-2-\log_2 s}$, represent the number of bit per segment. So, if we can hold the i^{th} segment initial amplitude coefficient c_i at the last clock cycle of the present segment interval , then we can easily derived the segment slopes coefficient m_i, at the first next clock cycle of the next segment interval. Fig 2 Shows the Simulink Model of the proposed DDFS.

During the present segment interval $Tseq_i$, The Register continuously latches the previous sample c_{i-1}, so, the inputs of the subtracter provide by c_i which is directed from ROM data bus and c_{i-1} from the output of register. At the first clock cycle in the next segment interval $Tseq_{i+1}$ the enabling signal En, enables the register to provide the delayed coefficient c_i at its output. The output remains unchanged during the new present segment interval. , consequently the data inputs of subtracter will be updated with the new coefficients c_i and c_{i+1}.

The En signal generated by the digital comparator which is simultaneously examines the ROM address bus for detecting the changes in data select inputs.

ROM LUT has s coefficients, so if we want to derive the slope correctly ,we have to prevent skipping segment and we have at least one clock cycle per segment, so the derivation process is valid as long as

$$1 \le \frac{2^{M-2-\log_2 s}}{FTW} \tag{4}$$
$$FTW \le 2^{M-2-\log_2 s}$$

Take into account that the output frequency $f_{out} = (FTW/2^M) f_{clk}$ leads to maximum frequency of

$$f_{max} = \frac{2^{M-2-\log_2 s}}{2^M} f_{clk} \tag{5}$$
$$= (2^{-2-\log_2 s}) f_{clk}$$
$$= f_{clk}/4s$$

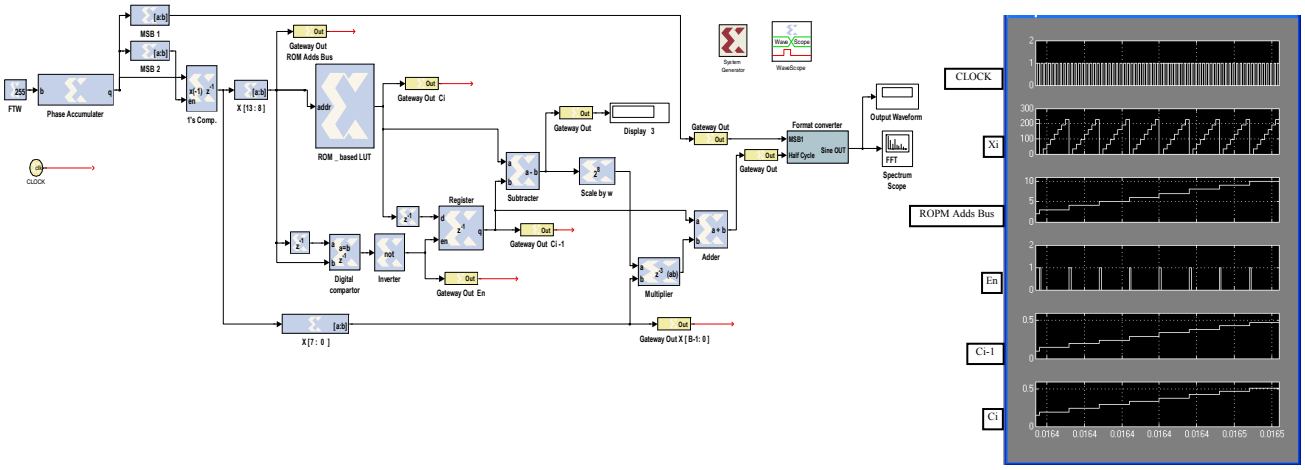

Fig. 2 .The proposed DDFS Model.

For practical consideration, the DDFS can only generate frequencies up to $f_{clk}/4$; the constraint comes from the sampling theorem, and that mean the proposed design has 1/s normal band width.

Hence, there is a trade-off between the improvement of SFDR level and the widening of band width where the SFDR level directly proportional to the number of segment [9].

$$SFDR = 24dBc + 20\log s^2 \tag{6}$$

Under this constraint, the proposed DDFS is suitable for high SFDR, narrow-band signal application. The application includes data encoding and signal-generator network analysis where the typical frequencies used in these applications tend to be from 0 kHz to 200 kHz [10].

And of special interest are applications based on hybrid PLL/DDS solution where the tuning resolution of the DDFS can enhance the tenability of the overall system to a level not possible with a PLL alone [10].

3. Simulation Results & Discussion

Based on the concept introduced in the previous section, we have designed a DDFS with 16-bit phase resolution and 64 piecewise linear segments. The DDFS was analyzed using MATLAB Simulink at the system level.

According to (6), architecture with 64 piecewise linear segments has worst case spur of -96 dBc. Figure 2 shows a MATLAB Simulink model of DDFS, where A is 6-bit length, B 8-bit length and P 15-bit amplitude resolution, yields to total memory size of ($2^6 \times 14$= 896 bit). The resultant architecture exhibited a 256:1 compression ratio.

Figure 3 shows the DDFS spurious level and their corresponding output waveforms of 61 KHz, and 1.945 MHz with 0.5GHZ clock frequency when the FTW is set to be 8, and 255 respectively. The results indicate an SFDR of about 96 dBc over the interest range; this is in line with the theoretical upper bound introduced in [9].

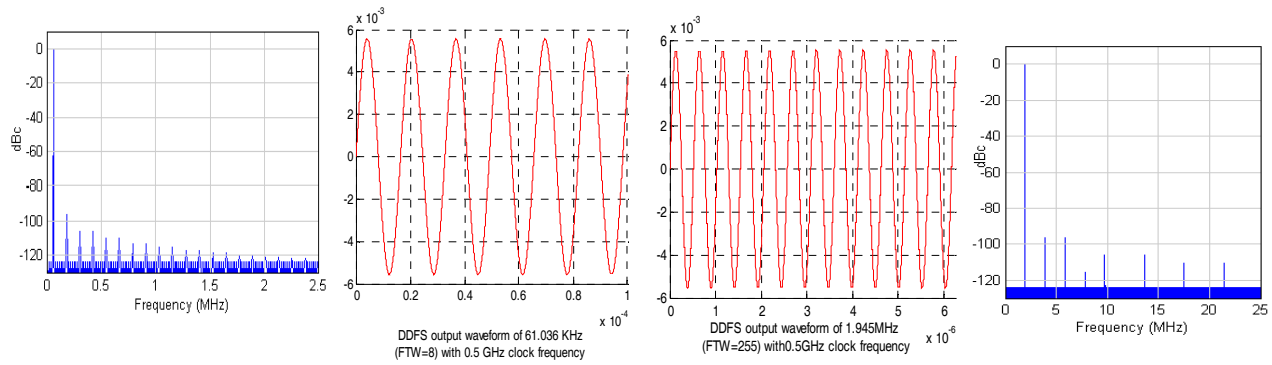

Fig. 3 DDFS spurious level and their corresponding output waveforms.

4. Conclusions

A new linear interposition technique was presented for application in high spectral purity narrow-band DDFSs. Only 64 points LUT with 6 bit digital comparator and one subtractor are required .System complexity is greatly reduced by using an efficient PSAC architecture. It was shown that a Compression ratio of 256:1 was attained. The proposed DDFS has been observed and tested over the interest frequency range. The spurious free dynamic range of synthesized sinusoid achieved 96 dBc which is adequate for many recent communications systems.

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