

# Evaluation of Low Power Carbon Nanotube Field Effect Transistor (CNFET) Master-Slave Latches

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**Abstract.** This paper presents evaluation and analysis of Master Slave Latches using Carbon Nanotube Field-Effect Transistors (CNFETs). Four different Master Slave Latches are implemented. Circuit performance of CNFET latches have been compared to silicon based CMOS latches in terms of Clk-Q delay, average power, power delay product (PDP), setup time and area. CNFET Master Slave Latches have shown superior performance over CMOS latches in simulations for most performance parameters.

**Keywords:** low power, carbon nano-tubes, Master Slave Latches, Flip-Flops

## 1. Introduction

Power consumption of VLSI circuits has increased substantially with the increase of speed and number of transistors per unit chip area. Power has become an important design constraint along with area and speed in modern VLSI design. Power consumption of digital CMOS circuits can be represented by the following equation:

$$P = \alpha C_L V_{dd}^2 f + I_{sc} V_{dd} + I_{leak} V_{dd}$$

Dominating this power equation is the first term, dynamic power consumption, which is due to logic switching. Here  $C_L$  is the load capacitance,  $\alpha$  is the switching activity,  $V_{dd}$  is the supply voltage, and  $f$  is the switching frequency. The second term is the power dissipated due to the short circuit current,  $I_{sc}$ , generated when both NMOS and PMOS transistors are simultaneously active. The last term is due to leakage current,  $I_{leak}$ , which varies with processing technology.

An effective way to reduce power consumption is to lower the supply voltage level of a circuit. Since voltage is quadratically related with dynamic power, a small reduction in the supply voltage results in a moderate reduction in the dynamic power consumption. Note, however, that the reduction in the supply voltage causes an increase in the circuit delay and consequently a reduction in the throughput. There are many obstacles that need to be addressed for the circuits to operate at low voltages.

Another well-known method to reduce power consumption is to reduce the size of the transistors. Sizing down the transistors decreases load capacitance ( $C_L$ ) linearly, and thus decreases dynamic and leakage power linearly [1]. It has been proposed that theoretically optimal minimum energy circuits use minimum sized devices [2].

In this paper designed Master Slave Latches will be designed using CMOS and CNFET technology parameters with transistor sizes are as small as possible to achieve low power.

## 2. Overview of the CNFET Structure

CMOS technology is approaching its limits and Carbon Nanotubes (CNTs) are considered as great candidate for future CMOS circuits because of their superior device performance and size advantage. CNTs

can be used to develop Carbon Nanotube Field Effect Transistors (CNFETs) whose conducting channel is made of carbon nanotubes. CNFETs intrinsic delay ( $CV/I$ ) is very low, show higher electron mobility compared to bulk silicon [3] and can provide better energy-delay product. CMOS circuit blocks can be realized using CNFETs since their operation principle is similar.

Although CNFET circuits show some imperfections such as misalignments, diameter and doping variations, improvements on CNFET device technology is promising. The Stanford University CNFET Model is a circuit-compatible, compact model for the intrinsic channel region of the MOSFET-like single-walled carbon-nanotube field-effect transistors [4,5,6]. CNFETs are about two to ten times faster, the energy consumption per cycle is about seven to two times lower, and the energy-delay product is about 15–20 times lower than silicon CMOS devices [6].

In this paper a promising alternative to silicon CMOS transistors, Carbon Nano-Tube Field Effect Transistors (CNFETs) will be used to implement master-slave latches. Performance of CNFET Latches will be evaluated using 32nm CNFET spice model [6]. The results will be compared with conventional CMOS Latches designed using BSIM 32nm predictive model [7]. Delay, average power, PDP, setup time, and area of both technologies will be calculated. The suitability of CNFET for low power Latches will be examined.

### 3. Design Of Master Slave Latches

#### 3.1. CMOS Implementations

Flip-flops are major components of digital circuits. Four different master-slave latch-pairs have been used for the flip-flop design and optimized in terms of power. In all designs a minimum size inverter is used as a load. Clock frequency is chosen as 10Ghz for power calculations.

$C^2$ MOS Latch's [8] modified version is used for the first latch design (Fig. 1). BSIM 32nm predictive model has been used for simulation. Transistor sizes are chosen as small as possible to achieve the lowest power. In  $MC^2$ MOS Latch, width to length ratio is chosen 2 to 1 ( $W/L=64nm/32nm$ ) for the NMOS gates and 4 to 1 ( $W/L=128nm/32nm$ ) for the PMOS gates in the forward path to overcome the loading effect of the feedback path transistors. All feedback path transistors (12 of them) are in minimum size. The worst case clk-to-Q delay is 7.21ps resulting  $88.35 \times 10^{-18}J$  power-delay product (PDP) at 10GHz clock frequency.

PowerPC 603 MS Latch [9] is used for the second design (Fig. 2). Most PMOS transistors are twice the size of NMOS transistors achieving relatively symmetric output delay (clk-QHL=13.55ps, clk-QLH=11.67ps). PowerPC MS Latch consumes less power compared  $MC^2$ MOS latch since the design requires less number of transistors (clk generation is ignored). However, overall power-delay product of PowerPC latch is worse than  $MC^2$ MOS latch.

For the third design DSTC MS Latch [10] is used. All the PMOS transistors are the twice the size of NMOS transistors. The design requires only 10 transistors but resulted with the worst delay and power consumption overall. Complex circuit topology causes the loading capacitance of each transistor to be higher than other latches.

For the final master-slave latch design SSTC MS Latch is used. PMOS transistors are the twice the size of NMOS transistors excluding bus keepers and inverters to improve logic 1 output. All the NMOS transistors are the minimum size to achieve low power. Output is driven by NMOS transistors providing strong logic 0. Logic 1 is provided by the bus keepers and design suffers from high clk-to-Q LH (low-to-high transition) delay. Output fan-out capacity would be very limited for this design.

#### 3.2. CNFET Implementations:

Four master-slave latch circuits ( $MC^2$ MOS Latch, Power PC 603 MS Latch, DSTC and SSTC) are also implemented using CNFETs. Most of the design requires width to length ratio as 1 for carbon nano-tube PCNFET and NCNFETs since current driving capacity is the same for both transistors. Number of tubes is taken as 3 (minimum) and increased for the transistors requiring larger current driving capability.

Electronic Properties Similarly, in the first master-slave latch circuit ( $MC^2$ MOS Latch) the number of tubes are determined as 3 (minimum) to reduce the power consumption.  $MC^2$ MOS LATCH was consuming

one third of the power compared to that of CMOS version. Average power delay product reduced to 12.83aJ with set-up time also reduced to one third.

PowerPC CNFET LATCH use minimum number of tubes (3) achieves 4 times better speed, 3 times less power and 13 times better PDP compared to silicon CMOS version. CNFET PowerPC LATCH set-up time is one fourth of the silicon PowerPC LATCHs set-up time.

TABLE I. COMPARISON OF LATCHES FOR CMOS AND CNFET IMPLEMENTATIONS.

	C <sup>2</sup> MOS		PowerPC		DSTC		SSTC	
	CMOS	CNFET	CMOS	CNFET	CMOS	CNFET	CMOS	CNFET
Clk-Q (HL) Delay [ps]	4.19	2.51	13.55	2.79	25.02	12.37	7.12	9.51
Clk-Q (LH) Delay [ps]	7.21	2.19	11.67	3.02	31.62	17.96	16.49	15.1
Average Power @10GHz [ $\mu$ W]	15.5	5.46	14.4	4.58	18	13.22	13.66	19.18
Power Delay Product (PDP) [aJ]	88.35	12.83	181.5	13.3	509.7	200.4	161.2	236
Setup Time [ps]	15	5	12	3	16	10	15	11
# of Trans.	20	20	18	18	10	10	16	16
Total Width [nm]	1152	640	800	576	480	320	608	640

Similarly CNFET DSTC use minimum size transistors with minimum number of tubes. Speed of latch doubles with 60% reduction of PDP. Total area is also reduced 2/3 of the CMOS design.

CNFET SSTC performance does not change much compared to CMOS version. CNFET design requires weak bus keepers at the output. Therefore transistor lengths of bus keeper inverters are chosen twice the size of CMOS version to reduce the driving capacity. That resulted increased area and power consumption compared to CMOS version. However set-up time is improved from 15ps to 11ps. SSTC Latch is not a good choice for CNFET design since driving capacity of the CNFET transistors are high.

#### 4. Conclusion

We compared performance of Master-Slave Latches for silicon based CMOS and carbon nano-tube CNFET devices. The results are summarized in Table 1. Overall MC<sup>2</sup>MOS Latch achieved the best speed and power performance but has little set-up time disadvantage compared to CNFET Power PC 603 MS Latch.

CNFET LATCHs show superior performance compared to CMOS LATCHs. CNFET LATCHs are up to 4 times faster, consumes 2-3 times less power and requires much less set-up time compared to CMOS LATCHs. Note that hold-time is 0 for all the designs. Power delay product of CNFET LATCHs are up to 14 times better than CMOS LATCHs which is similar to previous research results in literature[6]. Area reduction is up to 45% for the best case.

## 5. References

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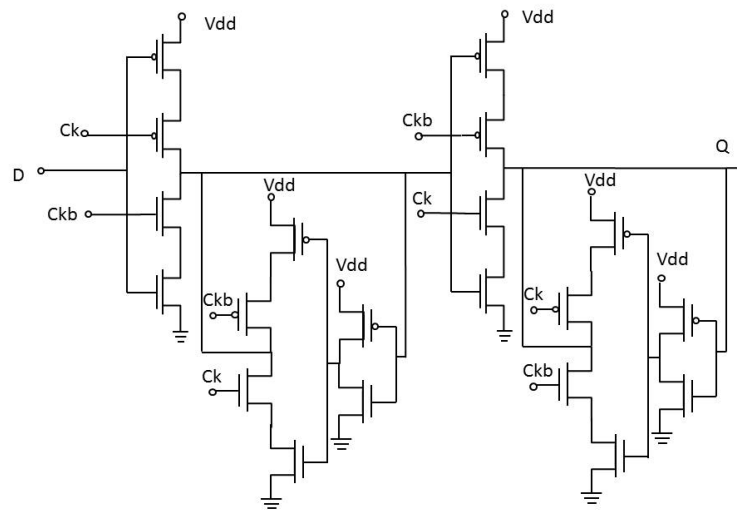


Figure1. MC2MOS Latch

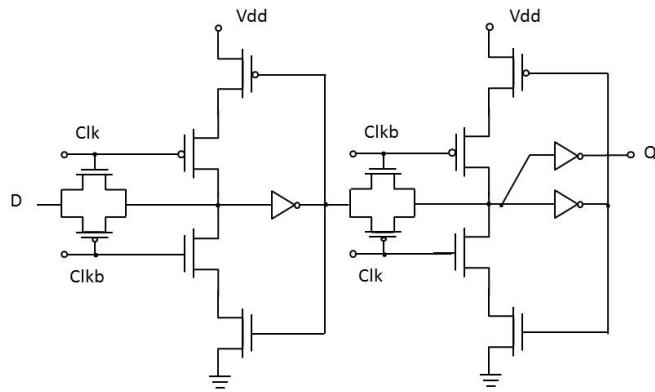


Figure2. PowerPC 603 MS Latch

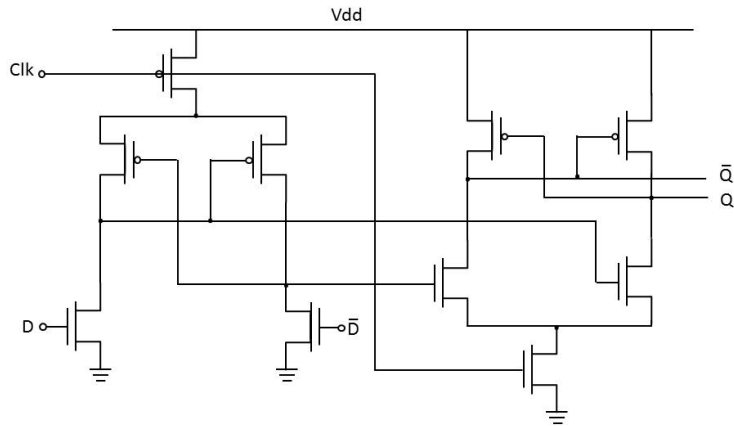


Figure3. DSTC MS Latch

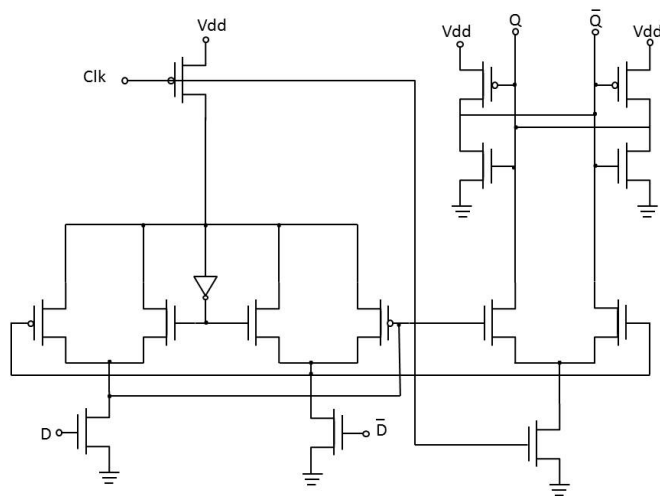


Figure4. SSTC MS Latch