# Evaluation of a silicon nanowire based thermoelectric cooler performance through contact processes considerations

Y. Li[1,2,3], K. Buddharaju[1, a)], N. Singh[1], S. J. Lee[2]

[1] Institute of Microelectronics, A\* STAR (Agency for Science, Technology and Research), Singapore

[2] Department of Electrical and Computer Engineering, National University of Singapore

[3] NUS Graduate School for Integrative Sciences and Engineering

**Abstract.** Contact resistance is a crucial part of any thermoelectric cooler design as it manifests in unwanted joule heating. Compared to bulk devices this resistance becomes much more significant in nanowire based thermoelectric devices due to the nano scale dimensions and should be considered while designing the device. In this work, electrical contact resistance between nanowire/metals system was extracted from fabricated test structures with nanowires of diameter 100nm. Firstly, the electrical contact resistances between silicon nanowires and three types of metallization scheme – Cu/Al, A-Si/Al, and TaN/Al were studied to develop a suitable metallization process. It was found that the lowest resistance was found in silicon nanowire/TaN/Al system. The results obtained were then used for a realistic evaluation of silicon nanowire based thermoelectric cooling using numerical simulations and modified thermoelectric analytical models.

**Keywords:** silicon nanowires, TEG, design

## 1. Introduction

The presence of high heat flux ($300Wcm^{-2}$ to $1000W/cm^2$)[1-3] in today electronics and optoelectronics is extremely detrimental to a circuit's performance and reliability. Hence, better cooling solutions will be needed to address such issues. Solution for such a problem can possibly be the integration of an embedded thermoelectric cooler Recently, a number of literatures has reported the merits of silicon nanowire (SiNW)in having an enhanced thermoelectric properties as compared to its bulk counterpart[4-6]. With the development of technology for the fabrication of SiNW, it can become a potential candidate in active cooling solutions in the near future.

Zhang et.al investigated the thermoelectric cooling performance of SiNW in both steady and transient state using numerical simulation.[7-8] The investigation however, neglected the presence of contact resistance as in an ideal case. Contact resistance is minimal in bulk material based TEC ($mm^2$ sized contact per thermoelectric leg[9]) and can be neglected in most cases. However in nanostructures, it is a sizeable portion of the overall resistance and cannot be underestimated.[10] High contact resistance will result in unwanted joule heating ($I^2R$) which will lower the maximum cooling possible in a thermoelectric device. Though there have been numerous reports on nanowires as thermoelectric devices all of them are more fundamental and material related which do not consider an integration perspective or the importance of a suitable back-end process.[4-6]

In this work, we attempt to address the effect of contact resistance in SiNW thermoelectric cooler system from a process perspective and propose a robust back end process such a system. Experimentally extracted values of contact resistance are then incorporated into numerical simulations to provide a more realistic value of cooling possible. A numerical simulation software, COMSOL MULTIPHYSICS[11] was employed to simulate and evaluate a single SiNW thermoelectric cooler with the inclusion of the experimental results. We

then also provided modified analytical models which incorporated the presence of contact resistance; the analytical and simulation results agree very well.

## 2. Experiment

SiNW arrays were fabricated on 8" silicon wafers using a CMOS top down approach. SiNW are defined through DUV lithography followed by DRIE etching.[12] Final SiNWs formed have an average diameter of ~ 100 nm, length of 1μm, and doped n-type to a concentration of ~1 x $10^{19}$ $cm^{-3}$ using Phosphorous ion implantation. This implantation step also connects the 2 SiNW arrays at the bottom. The SiNW structure fabricated has two groups of 100 SiNWs each where the nanowires are electrically connected in parallel within each individual group and each group is electrically connected in series with the other. In a real thermoelectric cooler there will be many such groups (of alternating groups of N doped wires and P doped wires connected electrically in series). But for contact resistance measurement we are considering just 2 groups with a single species dopant. Figure 1 (a) to (c) shows the schematic of the fabrication process. In this process the SiNWs were filled with silicon dioxide, which mimics a PMD in conventional CMOS technologies. Post contacts etch process we tried 3 different kinds of metallizations – Cu/Al, A-Si/Al, and TaN/Al. The purpose of the different metallization schemes is to determine the kind of metallization which provides a lower electrical contact resistance to the SiNWs. This metallization is the crucial part, which determines the contact resistance. In each of the metallization scheme, the rationale for the choice of material is based on its availability and compatibility to be used in current CMOS process technology; All contact processes described in this work employed standard CMOS –compatible semiconductor technologies.

Upon fabrication of the test structures, I-V measurements were taken to obtain the resistances at different locations across the wafer. In all the test structures fabricated, electrical I-V measurements were linear and indicated that ohmic contacts were formed between the SiNWs and the top metal. 20 data points were obtained of the resistances for the 3 different metallizations and shown in Figure 2. It was found that SiNW/TaN/Al system exhibited the lowest resistance variations among all. Taking the average resistance of the 3 metallizations scheme, we obtained the resistance values as Cu/Al – 378.5Ω, A-Si/Al - 256Ω, and TaN/Al – 253.5Ω. It can be seen that TaN/Al contact has a clear edge over others. In order to better quantify the contact resistance of the SiNW/TaN/Al, we fabricated another set of SiNW/TaN/Al test structure of 0.5μm long. Assuming that the contacts on both sets of SiNWs were identical due to the same process conditions used, the difference of the 2 sets of test structures resistance allowed us to calculate the resistivity of the SiNW. The resistivity of the SiNW was obtained as 4.67 x $10^{-3}$Ωcm, which agrees quite well with literature.[13] With the experimental SiNW resistivity, we calculated a range of actual contact resitivity ($\rho_{con}$) of the test structures to be in the range of 0.0184 to 0.191 μΩcm$^2$; with a mean value of – 0.0606 μΩcm$^2$.

In the following section, we will employ the range of $\rho_{con}$ obtained and simulate such effect on the thermoelectric cooling performance of a single SiNW thermoelectric cooler.
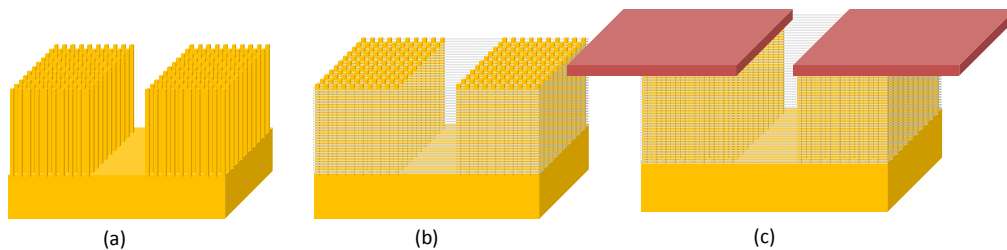


(a)          (b)          (c)

Fig.1: A schematic of the process of fabricating the test structures showing (a) SiNW array formation through DUV lithography followed by silicon dry etching process, (b) SiO2 (PMD) filling the air gaps between the SiNWs array to provide mechanical support and facilitate metallization, and (c) top metal depostion and etch to complete metallization. 3 different kinds of metallizations were used – Cu/Al, A-Si/Al, and TaN/Al.
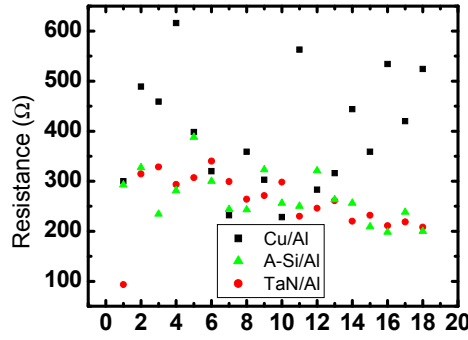
Figure 2: Range of data points (total resistance of test structures) obtained for the 3 different metallization schemes for 20 samples each. TaN/Al shows the least variations in resistance of test structure measured across the whole wafer

## 3. Simulation

Apart from the electrical characteristics of the SiNW obtained in our experiment, we made use of other thermoelectric properties of SiNW reported in literature for the simulation.[5,7] In short, we modeled a SiNW thermoelectric cooler with a 50nm x 50nm cross section contacted by Al metallization at its two ends. While the electrical parameters like SiNW resistivity and contact resistivity were taken from experimental results, the thermoelectric parameters adopted from literatures include the Seebeck coefficient (S) – 245µV/K, and thermal conductivity ($\kappa$) – 1.6 W/mK.[5] Since these parameters are mostly dependent on the material used (SiNW in this case), this is a valid adaptation. We made use of numerical simulation software, COMSOL MULTIPHYSICS[11] to study the steady state thermoelectric cooling phenomena of the SiNW. The governing equation for a thermoelectric cooler is given in Equation 1 [7].

$$\nabla.(-\kappa.\nabla T + S.T.J) = J.(-\nabla V) ---$$

(1)

where $J$ is the electrical current density and $V$ the electrostatic potential. In steady state, a temperature difference (dT) can be obtained across the SiNW upon constant application of an electric potential due to Peltier effect. This dT symbolizes the cooling that can be obtained from a thermoelectric cooler. By maintaing a constant temperature at one end of the nanowire the other end of the nanowire can be cooled accordingly. Based on this concept we simulated the thermoelectric cooling performance of the SiNW with the inclusion of varying electrical contact resistances. Figure. 3 (a) shows the steady state dT generated across the SiNW versus electric potential applied with varying $\rho_{con}$ as indicated in the legend.

It can be observed that the $\rho_{con}$ is an unwanted parasitic which will only serve to generate additional heat (joule heating) to be removed by the SiNW. Hence, the maximum dT attained by the SiNW decreased as the $\rho_{con}$ increased. In Figure 3(b), we plotted a graph that shows the heat flux which can be removed by the SiNW thermoelectric cooler with varying $\rho_{con}$. It should be noted that a constant electric potential of 0.07V (obtained from Figure 3(a)) was applied in all these simulations. The inset of Figure 3 (b) shows the maximum removable heat load by the SiNW thermoelectric cooler as $\rho_{con}$ vary. We define the maximum heat load removable as the heat load which resulted in the SiNW thermoelectric cooler having a dT of zero at 0.07V. Analytically, we can model the thermoelectric cooling with the inclusion of $\rho_{con}$ as per Equation 2.

$$\Delta T = \frac{-Q}{SI + \kappa\frac{A}{l}} + \frac{ST_H I - \frac{1}{2}I^2 R_{leg} - I^2 R_{con}}{SI + \kappa\frac{A}{l}} ---$$

(2)

where $R_{leg}$ is the SiNW resistance, $R_{con}$ is the electrical contact resistance between the SiNW and Al, $T_H$ is the hot junction temperature, and Q is the heat load applied to the cold side. The additional term of $I^2 R_{con}$

represents the Joule heating caused by the contact resistance. This analytical model matches very well with our simulation results as shown in the same graph of Figure 3(a) and (b). From these results it is evident that $\rho_{con}$ can be extremely detrimental to the cooling performance of a nanowire based embedded thermoelectric cooler. Hence, $\rho_{con}$ should be properly accounted for while designing a nanowire based thermoelectric cooler. Otherwise the benefits of a Si Nanowire over bulk (x100 lower thermal conductivity in SiNW`s over bulk Si) may be nullified by the mounting heating due to high contact resistivity . By proper optimization of the final metallization process this parameter can be kept at check to provide highly efficient thermoelectric devices.
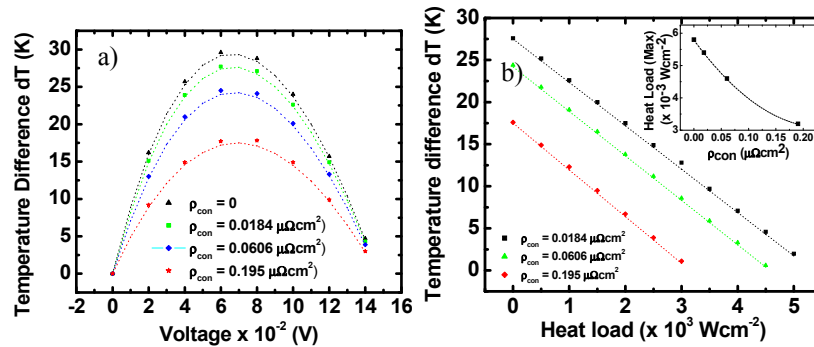


Figure 3: Steady state thermoelectric cooling simulation: dT across SiNW versus electric potential with varying $\rho_{con}$ and (b) dT across the SiNW versus heat load applied to the cold junction of the SiNW at an electric potential of 0.07V with varying $\rho_{con}$, Inset of Figure 3(b) shows the maximum removable heat load of the SiNW. Symbols represent simulated data while dotted line the analytical model.

## 4. Conclusion

In conclusion, we have investigated the suitability of different metallization contacts to SiNWs, namely, Cu/Al, A-Si/Al, and TaN/Al.It was found that the use of TaN/Al to provide metal contacts to SiNW resulted in the lowest electrical contact resistance. With the electrical contact resistance extracted from a SiNW/TaN/Al system, numerical simulation using COMSOL multiphysics on thermoelectric cooling was performed for a single SiNW thermoelectric cooler. The presence of the electrical contact resistance in a thermoelectric cooler resulted in a reduction of the maximum cooling effect due to parasitic joule heating. Analytical model was also presented which can predict the thermoelectric performance of the SiNW thermoelectric cooler very well. With careful design and optimization of contact processes to SiNW, we can expect extremely promising solutions for removing unwanted high heat flux  in numerous micro-electronic devices .

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