

HfO_x-Based RRAM Cells with Fully CMOS Compatible Technology

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Abstract: In this work, different HfO_x-based RRAM stacks, involving n⁺-Si, NiSi or Ni(Ge_{1-x}Si_x) bottom electrode which can be easily integrated with source/drain of a transistor, are systematically investigated. It has been found that the involvement of Ni (or NiO_x formed) in the stack is very beneficial to good switching properties. More importantly, RESET current can be effectively reduced for silicide electrodes as compared with n⁺-Si case, attributed to the formation of thicker interfacial layer involving NiO_x and/or GeO_x. Also, a well-controlled interfacial layer is found to be very helpful for the switching uniformity improvement. At the end, a highly manufacturable process with the above-mentioned RRAM cells localized at the bottom of a contact hole is proposed, suggesting the prospect of a more compact and CMOS friendly 1T-1R integration scheme.

Keywords: HfO_x, NiSi, Ni(Ge_{1-x}Si_x), RRAM, 1T-1R, 1D-1R, CMOS compatible integration scheme

1. Introduction

To overcome technological challenges faced by current flash memory, transition-metal-oxide (TMO) based resistive random access memory (RRAM) cell has been investigated extensively owing to its superior performance and CMOS compatibility [1-14]. In order to eliminate the cross-talk interference from neighboring RRAM cells, a selector, implemented either by 1D (diode) or by 1T (transistor), is required in each cell, wherein 1D-1R (RRAM) cross-bar architecture has been proposed for high density 3-dimensional (3D) integration [2]. However, the requirements for the diode selector, including high forward current density, high on/off current ratio, low processing temperature and high CMOS compatibility, have been found to be very difficult to be met simultaneously [3]. Therefore, the 1T-1R architecture still remains a valid option [8]. Apart from the type of selector device to be used in tandem with the RRAM, the material system involved in the RRAM cell needs to be explored further for high density and low cost application.

In this work, different HfO_x-based RRAM stacks, involving n⁺-Si, NiSi or Ni(Ge_{1-x}Si_x) bottom electrode, which can be easily formed on the source/drain (S/D) of a transistor, are systematically investigated. It has been found that the involvement of Ni (or NiO_x formed) in the stacks is very beneficial to good switching properties and more importantly, RESET current can be effectively reduced for silicide electrodes as compared with n⁺-Si case, attributed to the formation of thicker interfacial layer involving NiO_x and/or GeO_x. Also, a well-controlled interfacial layer was found to be very helpful for the switching uniformity improvement.

2. Device Fabrication

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Eight-inch n-type bulk Si wafers were first doped with As ($1 \times 10^{15} \text{ cm}^{-2}$ / 30 keV / 7° tilt) and activated at $1000^\circ \text{C}/10 \text{ s}$ in order to reduce series resistance from bottom electrode contacts as well as to mimic the formation procedure for S/D contact. After that, $\sim 50 \text{ nm}$ $\text{Ge}_{1-x}\text{Si}_x$ films with variable x were deposited selectively by Anelva Epi tool after surface clean. Then, 15 nm Ni was also selectively sputtered by physical vapor deposition (PVD), followed by a 2-step rapid thermal annealing (RTA) process flow (RTA1: $300^\circ \text{C}/30 \text{ s}/\text{N}_2 \rightarrow$ un-reacted Ni removal in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ solution \rightarrow RTA2: $450^\circ \text{C}/30 \text{ s}/\text{N}_2$) to form $\sim 30 \text{ nm}$ NiSi or $\text{Ni}(\text{Ge}_{1-x}\text{Si}_x)$ bottom electrode (BE). Subsequently, $\sim 10 \text{ nm}$ HfO_x film, with or without $\sim 1 \text{ nm}$ Ni capping layer, and $\sim 50 \text{ nm}$ TiN top electrode (TE) were deposited sequentially in PVD tool without breaking vacuum. Next, square-shape RRAM cells were patterned with lithography and dry etched. Finally, a low temperature ($\sim 400^\circ \text{C}$) back-end metallization process using Al was done to complete the device fabrication. Cross-sectional RRAM stacks are schematically shown in Fig. 1 and detailed information for all related samples in this work is summarized in Table I.

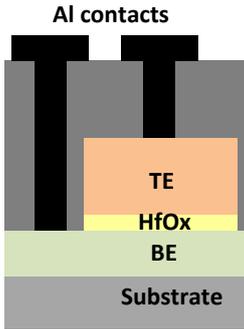


Fig. 1 Schematic illustration of RRAM stacks as device fabrication.

Table I: Summary of stack information and sheet resistances of BE for the investigated samples.

Sample ID		S01	S02	S03	S04	S05
TE	50nmTiN	V	V	V	V	V
	1nm Ni		V			
10nm HfOx		V	V	V	V	V
BE	n^+ -Si	V	V			
	NiSi			V		
	$\text{Ni}(\text{Ge}_{0.2}\text{Si}_{0.8})$				V	
	$\text{Ni}(\text{Ge}_{0.4}\text{Si}_{0.6})$					V
R_s (Ω/\square)				~ 3.6	~ 4.1	~ 4.7

3. Results and Discussion

Material/Physical Properties of RRAM Stacks The sheet resistance (R_s) of Ni silicide and germanosilicide layers was evaluated by using a four-point probe and is shown in the last row of Table I. The obtained low R_s indicate that mono-silicide, NiSi and mono-germanosilicide, $\text{Ni}(\text{Ge}_{1-x}\text{Si}_x)$, were formed without agglomeration or phase transformation [15], which is further confirmed by X-ray diffraction (XRD) analysis shown in Fig. 2(a). In addition, x in $\text{Ni}(\text{Ge}_{1-x}\text{Si}_x)$ was verified by X-ray photoelectron spectroscopy (XPS) to be around 0.6 and 0.8. It can be seen that the XRD spectra of $\text{Ni}(\text{Ge}_{0.2}\text{Si}_{0.8})$ and $\text{Ni}(\text{Ge}_{0.4}\text{Si}_{0.6})$ films are quite similar to those of NiSi, suggesting that Ge did not change the bulk properties of the silicide. Therefore, the difference of R_s among the films is believed to be due to the different amount of SiGe grains present in the silicide films [16].

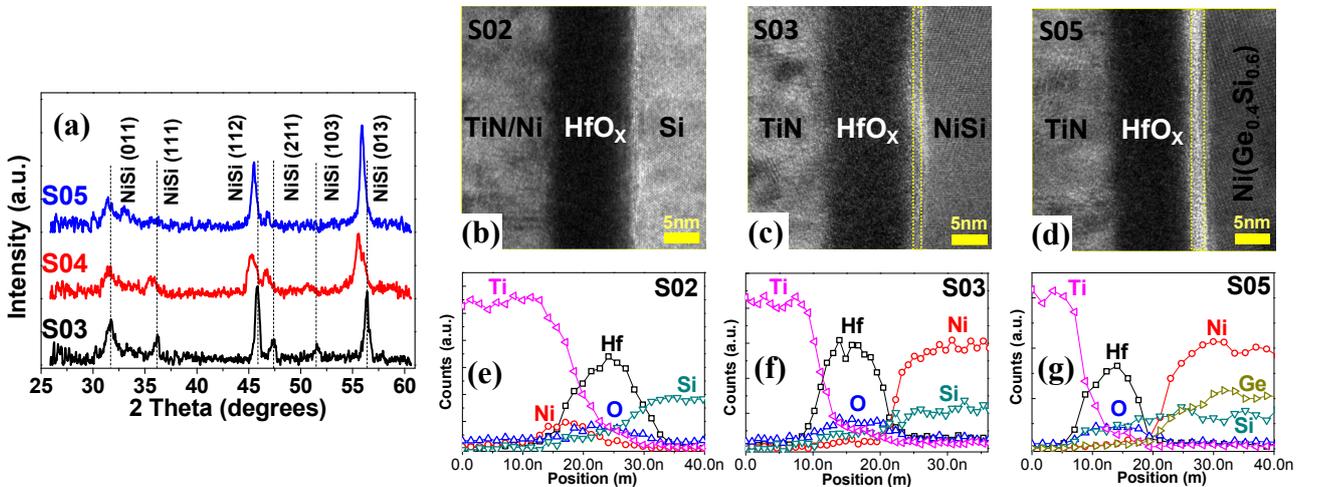


Fig. 2: (a) XRD spectra of BE layers used in S03, S04 and S05, indicating the formation of NiSi and $\text{Ni}(\text{Ge}_{1-x}\text{Si}_x)$ after the 2-step RTA process; (b-d) HRTEM images for S02, 03 and S05 and (e-g) their EDX line scan results, suggesting the formation of thicker oxide layer for $\text{Ni}(\text{Ge}_{0.4}\text{Si}_{0.6})$ as compared to NiSi and n^+ -Si BE cases.

The cross-sectional high-resolution transmission electron microscopy (HRTEM) images of S02, S03 and S05 shown in Fig. 2(b-d) reveal that all HfO_x layers are amorphous and have a thickness of $\sim 10\text{nm}$, as designed. The $\sim 1\text{nm}$ Ni capping layer on top of HfO_x in S02 cannot be identified due to the surface roughness of HfO_x . In addition, it is worth to note that S05 with $\text{Ni}(\text{Ge}_{0.4}\text{Si}_{0.6})$ BE and S03 with NiSi BE show an obvious interfacial layer ($\sim 1.8\text{nm}$ & 1.2nm respectively), as compared to S02 with n^+ -Si BE case. Their corresponding energy-dispersive X-ray spectroscopy (EDX) results shown in Fig. 2(e-g) first confirm the existence of Ni in S02 in between HfO_x and TiN, and also point out the formation of oxide layer at the interface between HfO_x and BE, i.e. NiSi and $\text{Ni}(\text{Ge}_{0.4}\text{Si}_{0.6})$ in S03 and S05 respectively. **Electrical/Switching Properties of RRAM Stacks**

The electrical measurements were performed using Agilent B1500A and 4156C semiconductor parameter analyzers, and the area of measured square-shaped RRAM cells was $100 \times 100 \mu\text{m}^2$. Figure 3(a) shows typical unipolar switching current-voltage (I - V) characteristics using direct current (DC) sweep and key switching parameters during switching. First, to activate the fresh cells with high resistance states (HRS), a Forming process with a current compliance is needed, while it has been demonstrated that this process may not be necessary for thinner HfO_x cases [6]. The subsequent voltage sweep causes the abrupt decrease of current and the resistance switches back to HRS, which is defined as a RESET process. Then, another voltage sweep with a current compliance triggers the abrupt increase of current similar as the Forming process, and the resistance switches from HRS to low resistance state (LRS), which is denoted as a SET process. Afterwards, functional cells switch reversibly in between HRS and LRS following RESET and SET process alternately.

It is interesting to observe that S01 did not show any reversible switching behavior after a Forming-like process, in sharp contrast with S02-S05 which have the incorporation of Ni either above or below HfO_x layer, clearly suggesting the importance of Ni in the switching behavior. Moreover, there is no clear indication of Ni diffusion through the $\sim 10\text{nm}$ HfO_x layer from the EDX analyses. Therefore, we believe Ni or more likely NiO_x involvement at the interface is playing the key role for the unipolar switching behaviors. More specifically, the conductive filaments' formation and rupture are determined by reduction and oxidation reactions through the interfacial layer, corresponding to SET process: $\text{NiO}_x \rightarrow \text{Ni}$ and RESET process: $\text{Ni} \rightarrow \text{NiO}_x$ respectively [9].

Figures 3(b & c) summarize the switching parameters for all functional samples. It can be noticed that Forming voltage (V_{Forming}) for cells with NiSi and $\text{Ni}(\text{Ge}_{1-x}\text{Si}_x)$ BE is much lower as compared with the n^+ -Si BE case, which suggests that the oxide layer formed at bottom interface in S03-S05 degrades the quality of HfO_x layer more seriously than the case with Ni capping layer in S02. The SET voltage (V_{SET}) for all of them shows quite a similar distribution, which suggests SET process is most probably dominated by a local electric field around the interface. In addition, it is worth to highlight that RESET voltage (V_{RESET}), especially RESET current (I_{RESET}) can be effectively reduced for silicided BE cases in S03-S05 as compared with the n^+ -Si case in S02. This effect should also be related to the thicker oxide layers formed at the interface, which are supposed to provide more oxygen species for the oxidation reaction during RESET process. In addition, Ge can also be detected in the interfacial layer, indicating a chance of GeO_x , which has been demonstrated to have low defect formation energy so that oxygen deficient centers, i.e. oxygen vacancies (V_o), would be easily generated [17]. The released oxygen atoms would be very beneficial to the oxidation reaction of Ni filaments during RESET process. This could explain the further reduction of I_{RESET} after the incorporation of Ge into NiSi.

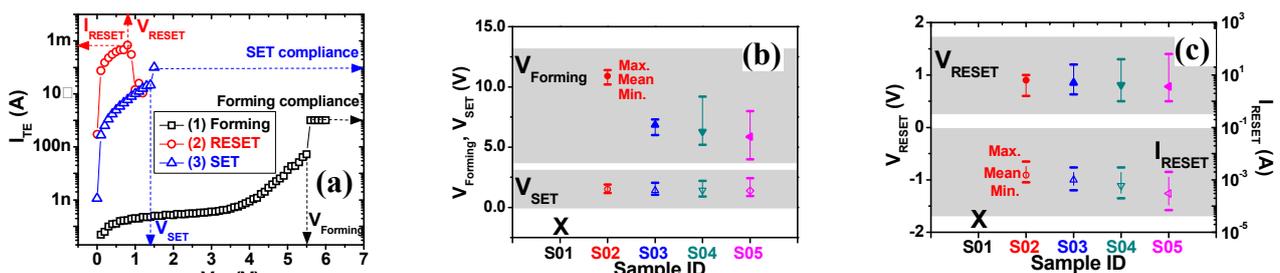


Fig. 3: (a) Typical switching characteristics extracted from S05, showing the Forming process, a consecutive RESET & SET switching curves as well as key switching parameters; Distributions of (b) V_{Forming} and V_{SET} and (c) V_{RESET} and I_{RESET} for S02-S05.

The reliability of the functional samples was then investigated. A typical cyclability of SET/RESET process with 100 cycles under DC conditions from S03 is shown in Fig. 4(a), where the resistances after SET (LRS or R_{ON}) and after RESET (HRS or R_{OFF}) as a function of the programming cycles are plotted. It can be seen that R_{ON} shows more stability than R_{OFF} , which confirms the filamentary property after the SET process or reduction reaction. On the other hand, it also indicates the variability of oxidation reaction during RESET process, which is dependent on available oxygen species and local temperature around the interface. R_{ON} and R_{OFF} distributions extracted from the similar test for S02, S04 and S05 are summarized in Fig. 4(b). Even though the incorporation of Ge into NiSi is beneficial to the I_{RESET} reduction possibly due to more released oxygen species around the interface, there is no clear improvement observed for the R_{OFF} distribution. This points out the importance of a controllable interfacial layer with uniform oxygen distribution for a stable RESET behavior, which has been experimentally demonstrated with a thicker GeO_x layer (7.5nm) in between Ni and HfON [10].

Retention properties for functional samples were also investigated. The cells were first heated up to a constant temperature, either 100°C, 150°C or 180°C, then programmed into LRS or HRS. After that, sampling measurements were carried out at 0.2V for each temperature point. In addition, the time to read error was determined when a significant change of resistance value occurred, ≥ 1 decade defined here. Figure 4(c) shows a typical test result on the stability of the LRS and HRS as a function of time at 100°C for S03. It can be noticed that the LRS presents longer read stability than the HRS state, and also both LRS and HRS tend to decrease with the time, which means the reduction reaction around the interface is more sensitive to the heat generated within the selected temperature range than the oxidation reaction. This can be explained by the increase of probability for V_o generation and oxygen ion mobility with the temperature increasing [4] so that NiO_x around the interface could lose oxygen more easily to form the filament or increase the filament size. The retention times for S02, S03 and S05 were extracted by considering the life time of HRS at different temperature points, and summarized in Fig. 4(d). It can be noticed that there is no big difference among the samples, and the projected retention time at room temperature is around 10^7 sec. A slight degradation of life time and projected retention time observed for S05 could be attributed to the lower defect formation energy (e.g. V_o) for GeO_x so that it is easier to form the filament or increase the size of filament.

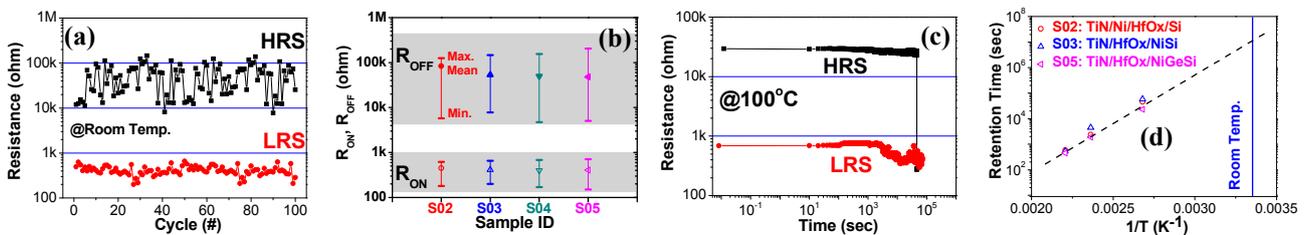


Fig. 4: (a) 100 cycles of SET/RESET processes under DC condition from S03, and resistance values at HRS (R_{ON}) and LRS (R_{OFF}) were extracted at 0.2V; (b) Summary of R_{ON} and R_{OFF} distribution; (c) Evaluation process of the life time for both HRS and LRS at 100°C from S03, and HRS shows relatively short life time; (d) Retention time projected from the life time extracted from HRS at different temperature points. Integration Scheme for the RRAM Stacks with CMOS Technology

Figure 5 illustrates an integration scheme for the above-mentioned functional RRAM stacks with CMOS technology, wherein the active RRAM stacks are formed directly at the bottom of S/D contact hole and the additional part out of the hole can be removed during the following chemical-mechanical polishing (CMP) process for tungsten plug formation.

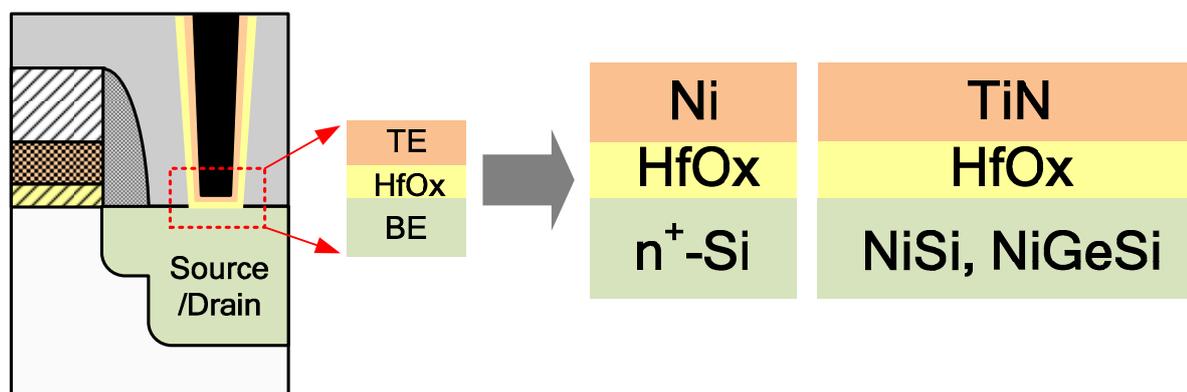


Fig. 5: The cross-sectional schematics of the 1T-1R unit cell, by integrating RRAM cells with S/D region of CMOS device directly.

4. Conclusion

Different HfO_x-based RRAM stacks, involving n⁺-Si, NiSi or Ni(Ge_{1-x}Si_x) BE were systematically investigated. It was found that the involvement of Ni (or NiO_x formed) in the stack was very beneficial to good switching properties and more importantly, I_{RESET} could be effectively reduced for Ni(Ge_{1-x}Si_x) as compared with n⁺-Si and NiSi BE, probably due to the formation of GeO_x. It was also inferred that a well-controlled interfacial layer was very helpful for the switching uniformity improvement. At the end, a highly manufacturable process with the above-mentioned RRAM cells localized at the bottom of a contact hole is proposed, suggesting the prospect of a more compact and CMOS friendly 1T-1R integration scheme.

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