

## A Fully Integrated 20-GHz Frequency Synthesizer in 0.13- $\mu\text{m}$ BiCMOS

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**Abstract.** This paper presents a fully integrated 20-GHz frequency synthesizer based on an integer-N fourth-order type-II phase-locked loop (PLL). The PLL synthesizer employing a cross-coupled  $LC$  VCO was fabricated in a 0.13- $\mu\text{m}$  SiGe:C BiCMOS process with a small chip area of 0.48 mm<sup>2</sup>. The VCO core current is 4 mA. The full tuning range of the VCO is 2.21 GHz from 19.9 to 22.11 GHz, and the PLL can synthesize output frequencies from 20.51 to 21.27 GHz. The phase noise at 100-kHz and 1-MHz offset frequencies from the carrier is -68.66 dBc/Hz and -97.17 dBc/Hz, respectively. The total power consumption of the synthesizer is 40 mW at a 1.5-V voltage supply. The frequency synthesizer can be used as a frequency source in highly-integrated wireless applications.

**Keywords:** frequency synthesizer, phase-locked loop (PLL), phase noise, frequency divider, voltage-controlled oscillator (VCO).

### 1. Introduction

Recently millimeter-wave (mm-wave) bands make it feasible for the wireless applications featuring high speed and high frequency, such as ultra-wideband communications at 60 GHz, automotive radars at 77 GHz, and imaging systems at 94 GHz. Attributed to constantly improving RF performances of devices, CMOS and BiCMOS technologies become great competitors of III-V technologies to implement the mm-wave systems with high performance, low power, low cost, as well as high integration.

As an essential building block of the mm-wave system, the phase-locked loop (PLL)-based frequency synthesizer is required to generate the frequency source, which is used to up convert the transmission data to the desired frequency band. Considering that it is still a challenging task of fully integrating high-performance frequency synthesizer on chip, the integer-N PLL generally becomes a principal candidate to realize the low-noise and low-power frequency synthesizer owing to its compact structure [1].

In this paper, we present a fully integrated 20-GHz integer-N frequency synthesizer implemented using only CMOS devices of a 0.13- $\mu\text{m}$  BiCMOS technology. When it is followed by a frequency multiplier, the frequency synthesizer can help generate mm-wave frequencies. The paper is organized as follows. Section II introduces the architecture and building blocks of the PLL-based 20-GHz frequency synthesizer. Section III presents the measurement results of the PLL-based frequency synthesizer. Finally, the paper is concluded in Section IV.

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## 2. PLL Building Blocks

Fig. 1 shows the architecture of the 20-GHz frequency synthesizer, which is based on an integer-N fourth-order type-II PLL structure. It consists of a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), a 20-GHz voltage-controlled oscillator (VCO), and a 1/256 frequency divider (FD) chain mainly constructed by 8-stage divide-by-2 dividers consisting of 3 stages of current-mode logic (CML) dividers and 5 stages of true single phase clock (TSPC) dividers. The reference and output frequencies are around 81.1 MHz and 20.76 GHz, respectively.

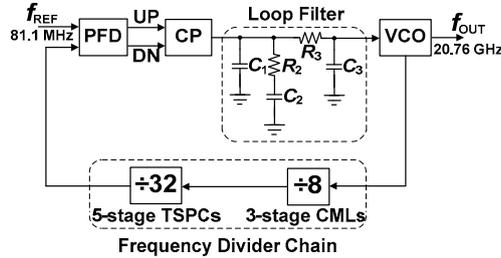


Fig. 1: Architecture of the 20-GHz frequency synthesizer.

### 2.1. PFD, Charge Pump and Loop Filter

Fig. 2 illustrates the schematic of the PFD [2], which is mainly realized by TSPC dynamic D flip-flops (DFFs). The reset path in the PFD is designed to effectively eliminate the dead-zone problem caused by the required time of turning on the charge pump. In order to compensate the delay discrepancy between output signals of UP and DN, a transmission gate is employed with a delay equal to that of an inverter.

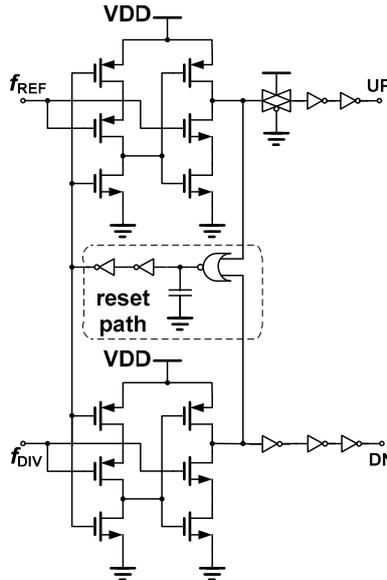


Fig. 2: Schematic of the phase-frequency detector (PFD).

The schematic of the CP [3] and LF is shown in Fig. 3. Switch transistors  $M_1$  and  $M_2$  controlled by UP and DN signals switch the current-source transistors  $M_3$  and  $M_4$  to charge up and down the output voltage  $V_{ctrl}$ ; current-source transistors  $M_3$  and  $M_4$  are designed in a way to moderate the charge injection and clock feedthrough to the output. Longer channel lengths are chosen for them to reduce the mismatch between the charge-up and -down current, which is designed to be 100  $\mu$ A at a  $V_{DD}$  of 1.5 V.

The LF is a third-order passive filter and fully integrated on chip. All capacitors are implemented by the vertical metal-insulator-metal (MIM) capacitors and the largest capacitor  $C_2$  is 24.3 pF with the acceptable chip area; resistors are realized by high-ohmic poly-Si resistors and the largest resistor  $R_3$  is 45.1 k $\Omega$ . The calculated phase margin is 56 $^\circ$  when  $K_{vco}$ , the gain of VCO, is 2.4 GHz/V.

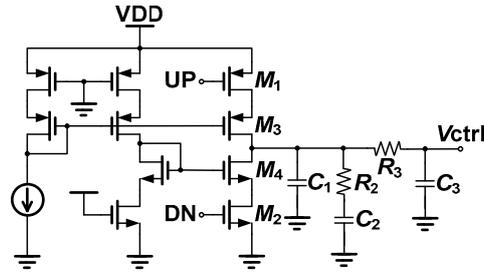


Fig. 3: Schematic of the charge pump (CP) and loop filter (LF).

## 2.2. Voltage-Controlled Oscillator (VCO)

The schematic of the cross-coupled differential  $LC$  VCO and buffers [4] is shown in Fig. 4. The VCO core is constructed by the cross-coupled nMOS transistors  $M_1$  and  $M_2$ , which yield the negative conductance to compensate the loss of the  $LC$  tank. Tail transistor  $M_3$  is used as the tail current source to set the current of the VCO. The  $LC$  tank is built by spiral inductors  $L_1$  and  $L_2$  together with MOS varactors  $C_1$  and  $C_2$ . Spiral inductors are generally designed to be high  $Q$ , by reducing the losses caused by the parasitic series resistance, featuring frequency dependence due to skin effect, and the parasitic shunt capacitance to the substrate. In order to achieve high  $Q$ , the inductors are shaped to be octagonal and symmetrical structure and implemented with the top-metal layer of 3- $\mu\text{m}$  thickness and at 10- $\mu\text{m}$  height from the silicon substrate. The width, space, inner diameter, and turns of the inductor are eventually optimized to be 7  $\mu\text{m}$ , 3  $\mu\text{m}$ , 50  $\mu\text{m}$ , and 1.5, respectively. The performance of the inductor is simulated with a full-wave 3-D EM high-frequency structure simulator (HFSS). The simulated inductance of the inductor is 150 pH and the  $Q$  is around 18 at the operating frequency of 20 GHz. The MOS varactors  $C_1$  and  $C_2$  are realized with a polysilicon-on-n-well structure, which has good linearity, high  $Q$ , and wide tuning ratio. The simulated tuning ratio  $C_{\text{max}}/C_{\text{min}}$  is around 3 at 20 GHz when the gate width ( $W$ ) and length ( $L$ ) of the varactor are selected to be 40  $\mu\text{m}$  and 0.3  $\mu\text{m}$ .

The output buffer of the VCO is a single-stage source follower amplifier, which features high input impedance to minimize the loading of the VCO core and low output impedance to permit the impedance matching to 50- $\Omega$  load.

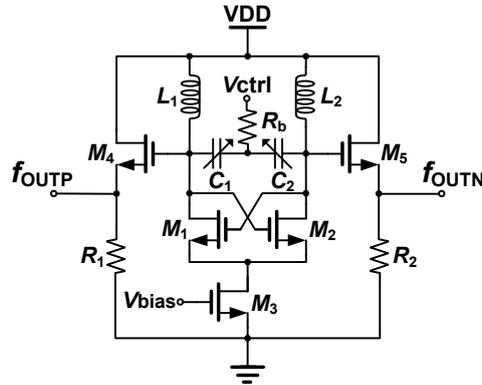


Fig. 4: Schematic of the voltage-controlled oscillator (VCO) and buffers.

## 2.3. Frequency Divider (FD) Chain

The output frequency of the VCO is around 20 GHz. A divide-by-2 static frequency divider is implemented with current-mode logic (CML) to achieve high-speed operation with small area as well [5]. Fig. 5(a) shows the schematic of the CML divider, which is built by a master-slave D flip-flop with the output nodes inversely connected to the input nodes. The master or slave includes an evaluate stage (differential nMOS transistors pair) and a latch stage (cross-coupled nMOS transistors pair). pMOS transistors in the evaluate stage replace the polysilicon resistors to act as loads since on-chip resistors in CMOS process are not controlled very well during fabrication. Compared with the conventional CML latches, the current sources are removed to obtain low-voltage operation. When no signals are applied to the input node, the master and slave latches allow signals to propagate through themselves, thereby operating as

a ring oscillator. The self-oscillation frequency is determined by the propagation delay, which is proportional to the RC constant at the output node. Large load transistors (pMOS) and small latches transistors (cross-coupled nMOS pair) lead to small RC constant so as to increase the self-oscillation frequency. Generally, higher self-oscillation frequency causes higher operating frequency of the divider. In the FD chain, 3-stage CML dividers are cascaded to exhibit the divide-by-8 characteristic; the first stage is designed to ensure that its maximum operating frequency is over the maximum frequency of the VCO with some margin and each stage can directly drive the next stage at its own operating frequency.

Note that the output of the last-stage CML divider must be converted to a full swing signal for the subsequent TSPC dividers. The CML-to-CMOS converter is shown in Fig. 5(b) [1], where the capacitor  $C_1$  is employed to AC-couple the input signal to  $INV_1$ , which is self-biased by the feedback resistor  $R$ , and the inverter  $INV_2$  is used as a buffer to ensure the rail-to-rail output signal to have sharp edges. The converter can work at high frequency with low-power consumption.

Since the output frequency of the last-stage CML divider is around 2.5 GHz, the TSPC dividers are employed to reduce the power dissipation. The 1/32 frequency divider includes 5 divide-by-2 TSPC stages. Fig. 5(c) shows the schematic of the divide-by-2 TSPC divider, which mainly consists of an edge-triggered D flip-flop with only 9 transistors [1]; the transistor parasitics are decreased to enhance the high-speed low-power operation.

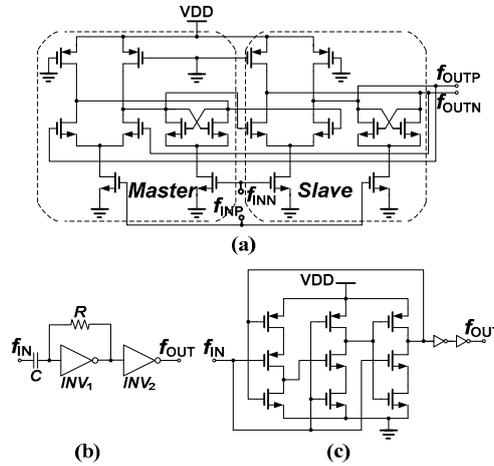


Fig. 5: Simplified schematic of the frequency divider chain. (a) CML static divider, (b) CML-to-CMOS converter and (c) TSPC divider.

### 3. Measurement Results

The frequency synthesizer has been designed and fabricated in a 0.13- $\mu\text{m}$  SiGe:C BiCMOS technology with a 7-metal backend. The nMOS transistors in the process achieve a cut-off frequency  $f_T$  of around 100 GHz and a  $f_{\text{MAX}}$  of around 130 GHz, respectively. The die microphotograph of the chip is shown in Fig. 6; the whole chip area including all testing pads is 0.84 mm  $\times$  0.57 mm. The single-end output of the synthesizer is designed as 50- $\Omega$  transmission line with top-metal layer of 15- $\mu\text{m}$  width to cancel out the pad and routing capacitance. On-wafer measurements were performed using Cascade 100- $\mu\text{m}$  ground-signal-ground (GSG) probes on a probe station. The input reference frequency ( $f_{\text{REF}}$ ) is provided by a HP 83712B signal generator and the output frequency ( $f_{\text{OUT}}$ ) is measured using an R&S spectrum analyzer. The total power consumption of the frequency synthesizer is 40 mW at a supply voltage of 1.5 V and the value is in good agreement with the simulation result.

Fig. 7 shows the measured tuning characteristic of the cross-coupled LC VCO versus the varactor control voltage ( $V_{\text{ctrl}}$ ). The tuning range is 2.21 GHz or  $\sim 10.5\%$  from 19.9 to 22.11 GHz when the  $V_{\text{ctrl}}$  changes from 0 to 1.5 V; the linear range is 0.96 GHz from 20.56 to 21.52 GHz while the  $V_{\text{ctrl}}$  varies from 0.6 to 1 V, thereby the linear gain of VCO is calculated to be 2.4 GHz/V. Since the  $Q$  of LC tank is dominated by the  $Q$  of inductor, a larger capacitance tuning range can be gained by increasing the finger length of the varactor. At the supply voltage of 1.5 V, the tail current of the VCO core is set to be 4 mA and the output buffers of

the VCO consumes around 14-mA current. The total current of the VCO determines the current of the synthesizer.

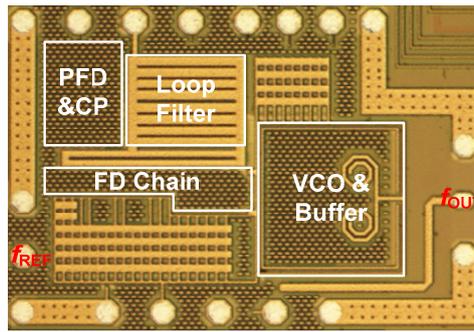


Fig. 6: Die microphotograph of the 20-GHz frequency synthesizer.

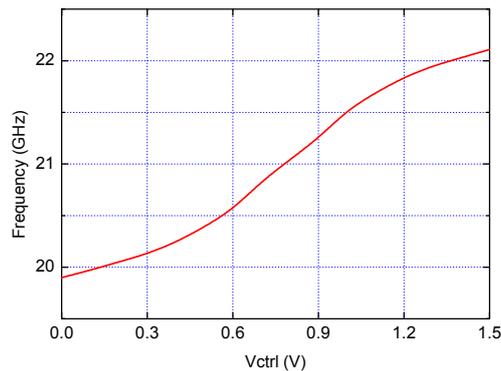


Fig. 7: Measured tuning characteristic of the cross-coupled *LC* VCO.

The output spectrum of the synthesizer is measured with 5-MHz span and shown in Fig. 8 when the synthesizer is locked. It can be observed that the output frequency is 20.76 GHz when the reference frequency is 81.1 MHz and the output power is  $-20.5$  dBm from which the cable and probe losses of  $-5$ -dB have not been deembedded. The output frequency is altered by tuning the reference frequency during the course of measurement. The synthesizer can be locked from 20.51 to 21.27 GHz when the reference frequency is changed from 80.1 to 83.1 MHz. The measured phase noise at the output frequency of 20.76 GHz is shown in Fig. 9. At 100-kHz and 1-MHz offset frequencies from the carrier, the phase noise is  $-68.66$  dBc/Hz and  $-97.17$  dBc/Hz, respectively. The output signal of the frequency synthesizer has low rms jitter of around 0.87 ps. Table I summarizes the measured performances of this work and compares them with those of other PLLs demonstrated previously.

#### 4. Conclusion

A fully integrated 20-GHz frequency synthesizer has been designed based on an integer-*N* fourth-order type-II PLL and implemented using a 0.13- $\mu$ m SiGe: C BiCMOS technology. The chip size is small, only 0.48 mm<sup>2</sup> including pads. The measured phase noise of the frequency synthesizer is  $-68.66$  dBc/Hz and  $-97.17$  dBc/Hz at 100-kHz and 1-MHz offset frequencies, respectively. The frequencies from 20.51 to 21.27 GHz can be successfully generated by the synthesizer. The whole synthesizer circuit has a power consumption of 40 mW at a supply voltage of 1.5 V. The demonstrated synthesizer has great potential to be used in highly-integrated wireless applications.

#### 5. Acknowledgements

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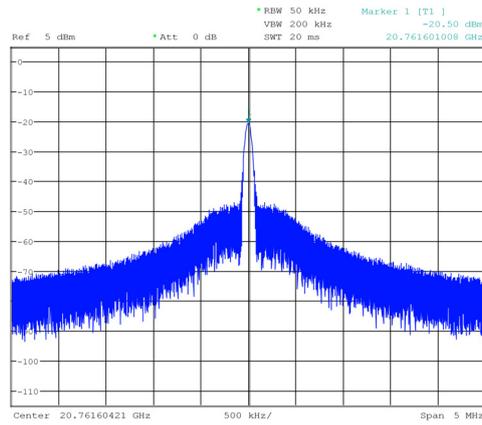


Fig. 8: Measured output spectrum at 20.76 GHz.

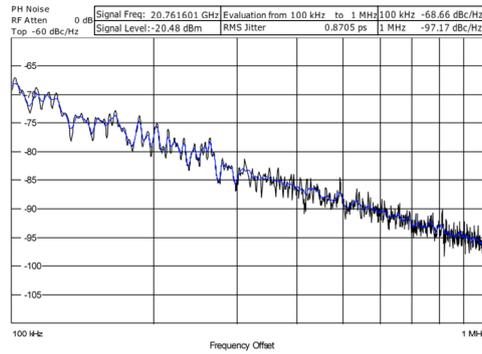


Fig. 9: Measured phase noise at 20.76 GHz.

TABLE I. Performance Summary and Comparison

References	[6]	[7]	This work
Technology	0.18- $\mu\text{m}$ CMOS	0.13- $\mu\text{m}$ CMOS	0.13- $\mu\text{m}$ BiCMOS
Architecture	Integer-N	Fractional-N	Integer-N
Supply Voltage (V)	1.5	1.5	1.5
Reference Freq. (MHz)	550~606	60	80.1~83.1
Output Frequency (GHz)	17.6~19.4	13	20.51~21.27
Tuning Rang of VCO	N.A.	8%	10.5%
Phase Noise (dBc/Hz)	-101.2	-100	-97.17
Power Dissipation (mW)	480	60	40
Chip Size ( $\text{mm}^2$ )	1.7	2.9	0.48

## 6. References

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