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N-channel Junction-less Vertical Slit Field-Effect Transistor (VeSFET): Fabrication-based Feasibility Assessment

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Abstract. The silicon implementation of junction-less Vertical Slit Field-Effect Transistor (VeSFET) fabricated on SOI wafer using conventional CMOS processes is presented. The twin poly-Si gates on the side walls of the vertical slit are defined using damascene process making them self-aligned and free from lithography restrictions on tall features. The NMOS transistors fabricated on 42 nm wide and 117 nm tall slit showed excellent electrical characteristics: I_{ON} = 20μA, I_{ON}/I_{OFF} ratio = 10^9, SS = 62mV/dec, DIBL = 13mV/V. The second gate could be used for providing better electrostatic control, threshold voltage tuning, or additional functionality.

Keywords: Junction-less, independent gate, Vertical Slit Field-Effect Transistor (VeSFET)

1. Introduction

Three-dimensional transistors, such as FinFET [1], tri-gate MOSFET [2], and gate-all-around (GAA) nanowire MOSFET [3, 4] have been researched extensively as solutions to short channel effects. Though promising from a scalability perspective, all these devices and their variants suffer from fabrication or reliability related issues. For example, the FinFET requires gate to be patterned across the fin and GAA nanowire MOSFET requires gate to be etched uniformly below the channel. Although some process challenges may be architecture specific, requirement of high depth of focus (DOF) is a common lithography issue with 3D devices, which is becoming more and more severe with advancement in lithography tools [5] – higher resolution at the cost of DOF. Three-dimensional devices also require doping to be conformal, increasing the complexity of junction formation, which, in any case, becomes more challenging with every new technology node [6]. Junction-less devices have started to gain research focus to tackle junction related issues [7-9]. As junction-less devices operate in depletion-mode – normally OFF due to depletion caused by gate work function and ON when depletion is removed by applying gate potential – the devices proposed in the past required the use of ultra-thin silicon-on-insulator (SOI) wafers, which may suffer from silicon thickness control, high extension resistance and other process complexities.

In this letter, we experimentally demonstrate a junction-less Vertical Slit Field-Effect Transistor (VeSFET), proposed by W. Maly, *et al*. [10-11], the schematic of which is shown in Fig. 1. It has its channel in the form of a vertical slit, with resistance modulated by two independent gates formed on the side walls to exhibit transistor action. Unlike conventional transistors, this device is free from doped-junctions, which generally cause speed degradation, unnecessary energy consumption, and increasingly difficult fabrication challenges with scaling. In addition, this device (a) is less expensive to fabricate due to lesser process steps, (b) has geometry that would reinforce maximum layout regularity, (c) can be fabricated with just circular patterns without requiring complex Optical Proximity Correction (OPC), (d) is 3D integration friendly due to

its vertical homogeneous nature such that access from both sides (top and bottom of the wafer) is possible, and (e) has no lithographic restrictions on effective channel widths, which is determined by the slit height. Furthermore, the independent second gate can be used for better electrostatic control, to tune the threshold voltage, or to get additional functionality [12].

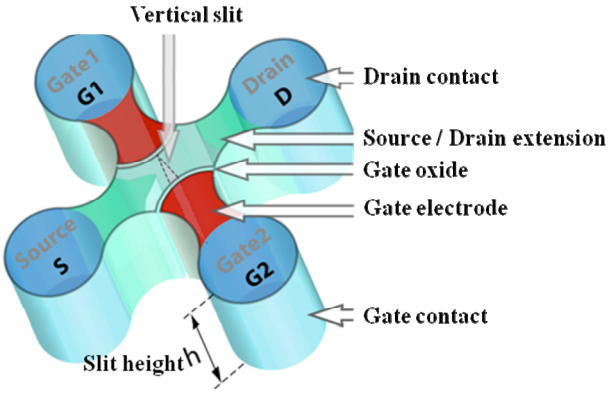

Fig. 1: Schematic drawing of junction-less VeSFET, with circularly-designed source/drain and gates that can be printed without complex OPC. The contact plugs to source /drain and gate can be through the top silicon to make the device vertically homogeneous and thus allowing interconnects from both sides.

In our first demonstration of an *n*-VeSFET presented here, we find the device exhibits excellent transistor characteristics (I_{ON} = 20μA, I_{ON}/I_{OFF} ratio = 10^9, subthreshold slope (SS) = 62mV/dec, DIBL = 13mV/V), which makes it suitable for future ultra-large scale integration.

2. Device Fabrication

VeSFETs were fabricated on standard 8" boron-doped (10^{15} cm^{-3}) SOI wafers with 117nm top silicon layer and a 145nm buried oxide. The scanning electron microscope (SEM) images of critical steps are presented in Fig. 2.

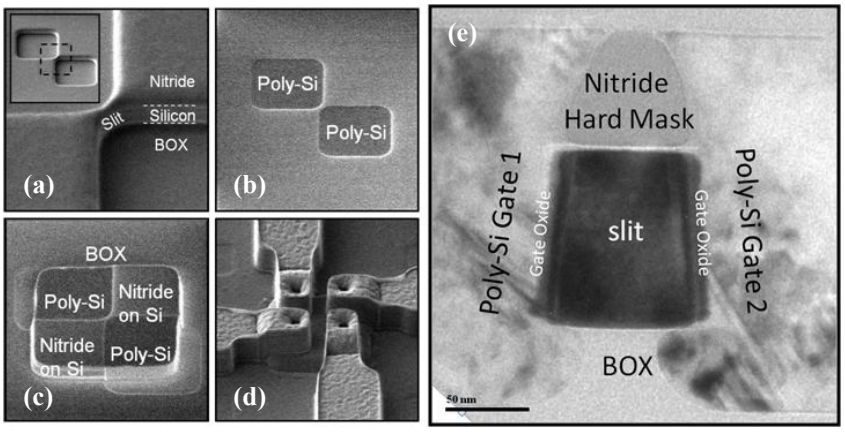

Fig. 2: Tilted SEM images after (a) nitride hard mask etch and silicon slit etch, (b) poly-Si gate CMP, (c) source/drain isolation etch and (d) metallization with four terminals. (e) Cross-sectional TEM image across a VeSFET device slit, showing the two independent gates on either side of the silicon slit.

Wafers were first implanted with phosphorus and annealed to yield uniform doping concentration of $5x10^{17}cm^{-3}$, the optimum concentration obtained through TCAD simulations for slit widths of 50nm; easily achieved using 200nm technology lithography tool. Silicon nitride was then deposited using low pressure chemical vapor deposition (LPCVD) process on a 3nm thermally grown pad oxide. Slits were patterned by deep ultraviolet lithography and etched into silicon nitride, which acted as a (1) hard mask for the actual

silicon slit etch, (2) stop layer for gate chemical mechanical polishing (CMP) and (3) ion implant blocking mask to stop dopants from entering into the channel during poly-gate implant. The underlying silicon was then dry-etched using nitride as hard mask. The SEM image after slit formation is shown in Fig. 2(a). To further reduce the slit width and to reduce the sidewall surface roughness of the slit, a layer of sacrificial oxide was thermally grown and subsequently removed by diluted HF wet etch. Gate oxide (4.5nm) was grown by dry oxidation, followed by deposition of LPCVD amorphous silicon as gate material. The deposited amorphous silicon on the top surface was removed by selective CMP until nitride hard mask was exposed to isolate the two gates as shown in Fig. 2(b). Gate was then implanted with BF_2 and activated, with the source/drain and channel slit protected by the nitride hard mask. Fig. 2(c) shows the formation of source and drain isolation by subsequent active area patterning and etching. A pre-metal dielectric oxide layer was deposited followed by contact hole etching and standard metallization processes.

To ensure ohmic source/drain contacts, the source and drain contact holes were patterned separately from the gate contacts and heavily implanted with arsenic. In these VeSFET devices, channel was *n* implanted while poly-gate was *p*+ implanted to make the devices normally OFF by work function tuning. Fig. 2(d) shows the SEM image of a fully-fabricated 4-terminal VeSFET (2 gates, 1 source and 1 drain) device. Fig. 2(e) shows the cross-sectional TEM image across a VeSFET device, showing its slit region as well as the two independent gates.

3. Results and Discussion

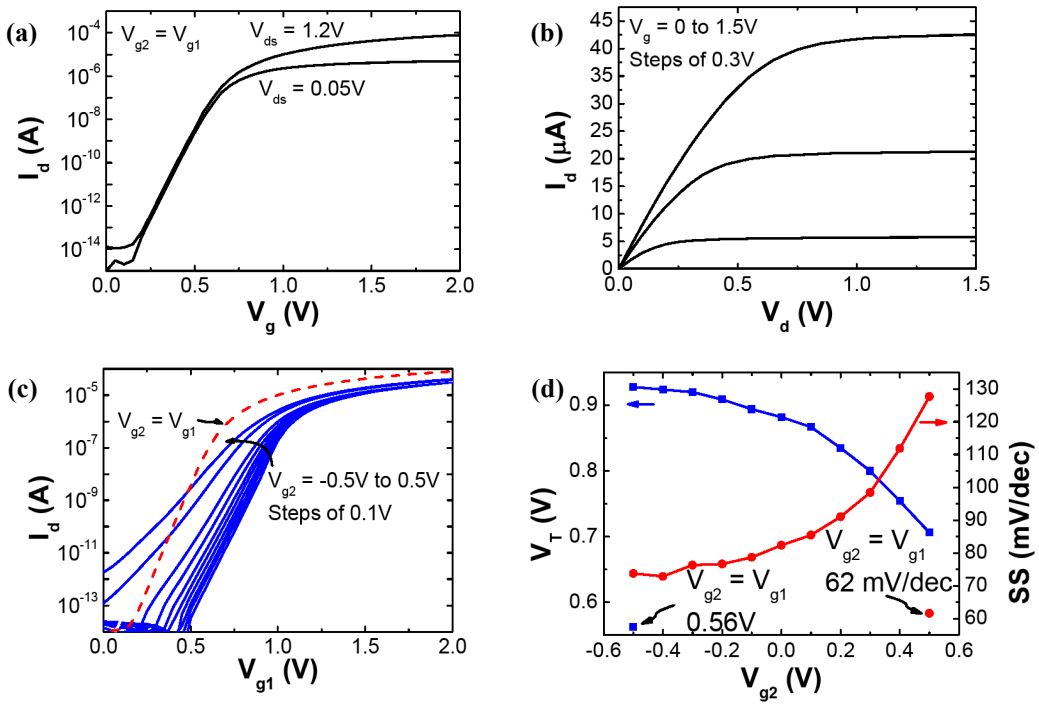

Fig. 3: (a) I_d-V_g and (b) I_d-V_d characteristics when both gates are swept together, showing no short-channel effects, (c) I_d-V_g characteristics when Gate 1 is swept while Gate 2 is biased (V_{ds}=1.2V). The red dotted line represents the I_d-V_g curve when both gates are swept together. (d) Threshold voltage (V_T) and SS variation when Gate 2 is biased. V_T extraction is through linear extrapolation method.

The VeSFET devices were characterized by applying different fixed potentials on one gate while sweeping the other gate, and also by sweeping both gates together to yield the transfer characteristics. Shown in Figs. 3(a) and 3(b) are the I_d-V_g and I_d-V_d characteristics (both gates swept together), respectively, for an n-VeSFET device with slit doping of $5x10^{17}$ cm^{-3}, slit width of 42nm, slit height of 117nm and gate oxide thickness of 4.5nm. Device shows near ideal turn ON with SS = 62mV/dec and DIBL = 13mV/V. I_{ON} of 20μA at V_g = 1.2V is obtained with OFF state leakage current as low as 10fA. These VeSFET devices, even

with nano-scale features (slit length ~ 100nm), do not exhibit velocity saturation effects as can be seen in the I_d-V_d curves (Fig. 3b) with near-perfect saturation and near-quadratic increase of drain current. This is due to enhanced gate electrostatic control at smaller slit widths and the additional arsenic source/drain implant through the contact hole which reduced the source/drain contact resistance [12].

Shown in Fig. 3(c) is the I_d-V_g characteristics with independent gate control exhibited. Gate 2 was biased in steps of 0.1V from -0.5V to 0.5V while Gate 1 was swept to yield each individual current transfer characteristic (blue solid lines). The red dotted line shows the transfer curve when both gates are swept together. The effects of biasing Gate 2 can be seen by the change in threshold voltage (V_T) and SS. This dependence of V_T and SS on Gate 2 bias can be seen in Fig. 3(d) demonstrating tunability of device parameters through gate bias. V_T can be modulated by biasing Gate 2, but with a trade-off with SS. Shorting both gates exhibits the highest saturation current and also yields the best SS of 62mV/dec because of the decrease in threshold voltage as well as the combined electrostatic contribution from both gates [13]. This can be seen in Figs. 3(c) and 3(d).

4. Conclusion

An *n*-type junction-less Vertical Slit Field-Effect Transistor (VeSFET) fabricated on SOI wafer using conventional CMOS processes was presented. The fabrication process was easy having self-aligned gate, without requiring complex lithographic patterning on tall 3D features or precise junction formation. Excellent transistor characteristics with high I_{ON} and I_{ON}/I_{OFF} ratio, near ideal SS and low DIBL were shown. Improvement in electrostatic control and tunability of threshold voltage were demonstrated using independent second gate. In addition, the VeSFET device architecture provides the capability to implement high density CMOS devices with high drive currents by simply increasing the device widths through slit height, with no area penalty unlike conventional planar transistors, making the device a suitable candidate for future ultra-large scale integration.

5. References

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