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Vertical Silicon Nanowire CMOS Inverter

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Abstract. Vertical Si nanowire (SiNW) gate-all-around MOSFETs with Ni-silicided nanowire tip is presented. The fabrication process is top-down CMOS compatible and is similar to previously reported vertical SiNW tunneling FETs (TFETs) where silicidation at the nanowire tip is done to segregate dopants at the channel interface for an abrupt junction. Also, for the first time, we demonstrate threshold voltage tuning through opposite doped poly-Si gate, ie. *p*+ poly-Si gate for *n*-MOSFET and *n*+ poly-Si gate for *p*-MOSFET. The devices exhibit fair performance (SS < 100mV/dec, $I_{on}/I_{off} > 10^7$) slightly degraded due to Schottky barrier formation. Most significantly, this work paves the way for future MOSFET/TFET integration.

Keywords: Gate-all-around (GAA), top-down, Ni-silicided, vertical silicon nanowire (SiNW).

1. Introduction

The gate-all-around nanowire architecture, with its enhanced gate electrostatic control, has the ability to go beyond the 22nm technology node [1-7]. The vertical nanowire platform further increases the device density with the possibility of stacking multiple gates on a single nanowire [4-8]. Non-conventional FETs also enjoy the many advantages of this platform, like the impact-ionization MOSFET [9] and the tunneling FET (TFET) [10-11]. However, the low drive current of TFETs may not be able to drive most circuits. This low driveability can be countered by integrating MOSFETs with TFETs, forming a hybrid circuit, with MOSFETs playing the role of providing high driveability and the TFETs keeping power low with its sub-60mV/dec sub-threshold swing.

The difficulty of MOSFET and TFET integration is the use of silicidation at the nanowire tip to segregate dopants at the interface to form an abrupt junction for TFETs. The effect of this process on the MOSFET is not known. Another problem is the low threshold voltage (V_T) of poly-Si gate SiNW MOSFETs not allowing circuit integration. Interestingly, the vertical SiNW TFET was found to have near-ideal V_T, which is attributed to the opposite doping employed during fabrication, ie. *p*+ poly-Si gate for *n*-TFET and *n*+ poly-Si gate for *p*-TFET. The work function difference between gate and channel, which largely determines V_T, correctly gives a suitable V_T value. This method of V_T tuning with gate doping has yet to be used in conventional vertical SiNW MOSFETs.

We present vertical SiNW MOSFETs fabricated in similar fashion as the vertical SiNW TFETs and employing V_T tuning via opposite gate doping and dopant segregation through silicidation at the nanowire tip. The devices show fairly good performance, with SS < 100 mV/dec and $I_{on}/I_{off} > 10^7$.

2. Device Fabrication

Fabrication was done on *p*-type (boron ~10^{15} cm^{-3}) Si-on-insulator wafers. Fig. 1 shows the process flow schematic, which is similar to [10-11] but with the final implants targeted to form MOSFETs instead of TFETs.

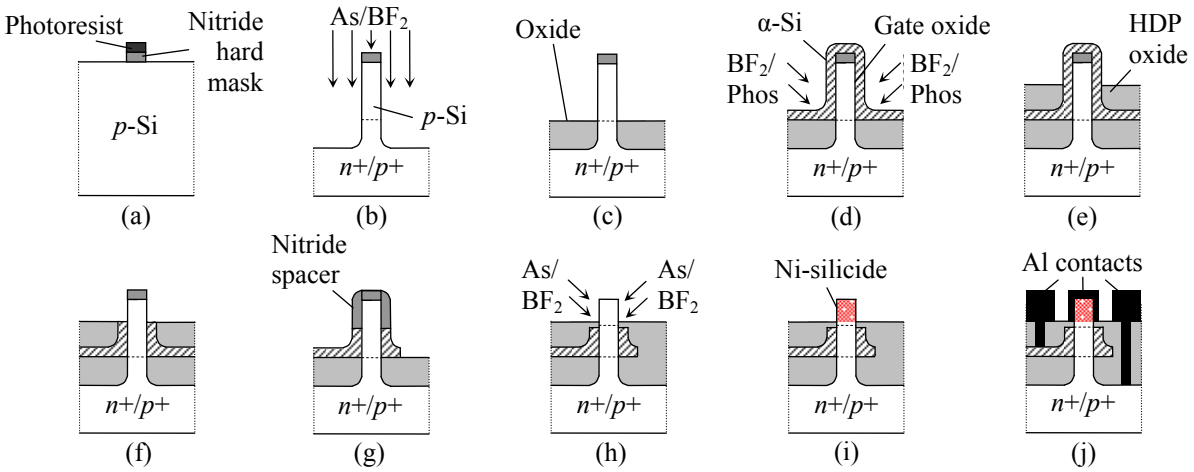

Fig. 1: Vertical Si nanowire MOSFET with Ni-silicided tip process flow. (a) Nitride hard mask etching, (b) Nanowire etching using deep reactive ion etching and vertical implantation of nanowire bottom. (c) high-density plasma (HDP) oxide non-conformal deposition and dilute HF (DHF) etch-back. (d) Gate oxide growth, α-Si gate deposition and implantation. (e) HDP oxide deposition and DHF etch-back. (f) Isotropic dry etching of α-Si tip, (g) formation of nitride spacer and oxide wet etching followed by gate patterning. (h) Nanowire tip implantation, (i) Ni deposition and two-step silicidation. (j) Aluminium contact formation.

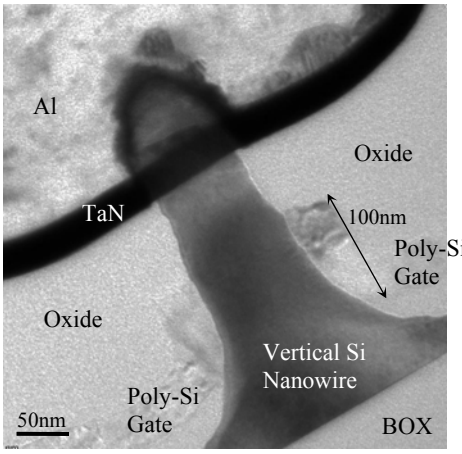

Fig. 2: Transmission electron microscope image of the vertical Si nanowire device with ~80nm diameter and ~100nm gate length.

After photoresist patterning of the nitride hard mask using deep-ultraviolet lithography and reactive ion etching (RIE) (Fig. 1a), vertical nanowires were defined through a deep RIE process and oxidation to reduce diameter and sidewall roughness. The bottom of the nanowire was implanted with As [$2x10^{15}cm^{-2}$/ 30keV/ 0° tilt] for *n*MOSFETs and activated [1050°C/10s] before the implantation of *p*MOSFETs [BF_2/ $2x10^{15}cm^{-2}$/ 20keV/ 0° tilt; activation 950°C/10s] as shown in Fig. 1(b). All implants were through implant masks to define *n*- and *p*-type regions. The isolation between the gate and bottom of nanowire was created by a non-conformal oxide deposition and wet etch-back process (Fig. 1c).

A 4.5 nm grown SiO_2 and 50 nm low-pressure CVD α-Si are then formed as the gate stack and the α-Si was doped with BF_2 for *n*MOSFETs and phosphorous for *p*MOSFETs [four orthogonal implants: $1x10^{15}cm^{-2}$/ 5keV/ 30° tilt], once again with implant masking, and activation done [950°C/10s] to form poly-Si (Fig. 1d). The oxide isolation process was repeated (Fig. 1e) and exposed poly-Si was isotropically etched in SF_6 plasma, defining the gate length (~100 nm). A silicon nitride spacer was formed, the isolation oxide stripped in dilute HF and the gate patterned using lithography (Fig. 1g). The nitride hard mask and spacer was then

removed in phosphoric acid and oxide isolation process repeated once more to expose the tip of the nanowire for implantation: As for *n*MOSFET and BF_2 for *p*MOSFET [four orthogonal implants: $1x10^{15}cm^{-2}$/ 10keV/ 60° tilt] (Fig. 1h). A two-step silicidation process follows: 15nm Ni deposition using PVD, annealing at 220°C for 120s, wet etching unreacted Ni in H_2SO_4:H_2O_2:H_2O solution, and finally annealing at 440°C for 30s (Fig. 1i). Metallization is a standard low temperature (<430°C) process using Al and TaN barrier (Fig. 1j).

Fig. 2 shows the transmission electron microscopy image of the fully fabricated vertical SiNW device showing a gate length of ~100nm with diameter ~80nm.

3. Results and Discussion

Fig. 3(a) shows the I_d-V_g curves of typical vertical SiNW *n*MOSFETs and *p*MOSFETs. Device performance is fair, with SS < 100mV/dec and $I_{on}/I_{off} > 10^7$. The non-linearity at low V_d indicates a Schottky barrier existing in the device. This could mean that although the silicidation segregates the dopants at the NiSi/Si interface to create an abrupt junction, the dopants may not be fully activated at the low temperature of 480°C. The low doped Si thus forms a Schottky barrier with the NiSi. A possible solution to this could be a rapid annealing of the dopants, either through spike annealing or laser annealing, to form a highly doped region before silicidation. However, this may cause the junction to lose its abruptness.

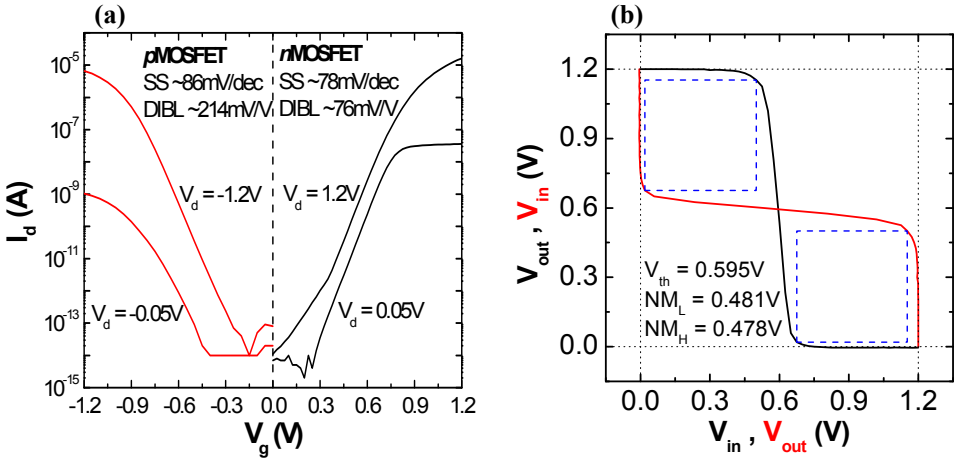

Fig. 3: (a) I_d-V_g plot or input characteristics of typical vertical Si nanowire *n* and *p*MOSFETs, and (b) the butterfly curve of the CMOS inverter formed by both the *n* and *p*MOSFET (V_{dd} = 1.2V).

Most significantly, due to the opposite gate doping, the work function difference between gate and channel regions is now large, thus pulling the V_T to the correct value. Thus, the $|V_T|$ is now positive (~0.8V), showing the tunability of V_T via gate doping which allows circuit integration. The circuit performance is evaluated using a CMOS inverter co-fabricated with the MOSFETs. Fig. 3(b) shows the CMOS inverter characteristics at V_{dd}=1.2V. At a higher V_d of 1.2V, the Schottky barrier is overcome and its effects are reduced, resulting in excellent inverter characteristics: V_{th} is ideal at 0.595V and noise margins are wide (NM_L = 0.481V, NM_H = 0.478V).

4. Conclusion

The vertical Si nanowire MOSFET with Ni-silicided top and oppositely doped gate poly-Si is presented. Device performance is fair with the formation of a Schottky barrier causing non-linearity at low V_d. However, the threshold voltage is now properly adjusted with gate doping and allows circuit integration. The inverter characteristics show good performance with ideal V_{th} and wide noise margins at V_{dd}=1.2V. Most significantly, this work paves the way for future MOSFET/TFET integration.

5. References

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