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An Independent Double-Gate Thin Film FinFET Featuring Lithography-Free Channel Length Definition

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Abstract. We present a novel approach to fabricate thin film FinFETs having two independent side gates, self-aligned source/drain junctions and lithography-free channel length definition. N-type inversion-mode devices with sub-100nm channel length are fabricated on poly-silicon films with silicon nitride isolation layer. The dual poly-Si gates on the side walls of the vertical channel are defined using a damascene process. Devices showed good electrical performance (I_{ON}/I_{OFF} ratio = 10^6, SS = 120mV/dec, DIBL = 150mV/V) and wide range of threshold voltage tunability. The proposed method can be directly implemented on SOI or bulk wafers to provide high performance devices and has high potential for fabricating vertically stacked circuits.

Keywords: Independent double gate FinFET, four terminal (4T), thin film, poly-silicon, lithography free channel length.

1. Introduction

Multi-gate devices have been researched for the last two decades to tackle scaling issues in planar CMOS transistors [1-2]. These devices can offer much more than just improved gate electrostatic control, provided the gates are controlled independently. Recently, independent gate control in FinFET has been used for dynamic threshold voltage control [3], enhancing SRAM cell performance [4-5], dynamic power management in logic circuits [6], and improved conversion gain and linearity in RF mixers [7]. However, the FinFET poses manufacturing challenges for lithography and etching due to its 3-dimensional structure; forming independent gates makes the process integration even more complex [8-9].

We present a novel method to fabricate an independent double-gate (IDG) inversion-mode FinFET. The device schematic along with cross-sections is shown in Fig. 1. It has a physical structure similar to a Vertical Slit Field Effect Transistor (VeSFET) [10-11]. The channel length is defined by nitride spacers that mask the fin during source/drain implant thus creating scaled channel length with symmetric source/drains junctions. It is therefore independent of lithography and can be precisely controlled by spacer deposition etching. This device structure is demonstrated by fabricating *n*-type FinFETs with sub-100 nm channel length on poly-silicon film. The devices showed good electrical performance and wide range of threshold voltage tunability. In addition to integration-friendliness, the presented device architecture and method are promising for fabricating thin film vertically stacked circuits.

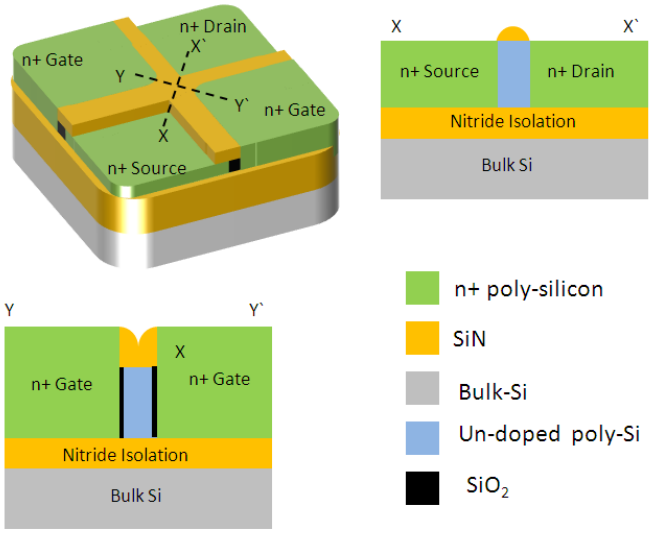

Fig. 1: Device schematic and cross-sectional views across and along the channel.

2. Device Fabrication

The fabrication was done on standard 8" bulk silicon wafers. Shown in Fig. 2 are the scanning electron microscope (SEM) images corresponding to the steps contributing to the physical architecture formation. A stack of silicon nitride (200nm), amorphous silicon (110nm), and silicon nitride (150nm) was first deposited using low pressure chemical vapor deposition (LPCVD) process. The bottom nitride acts as a device isolation layer, the amorphous silicon as active device layer, and the top silicon nitride as hard mask for etching the active device layer and stop layer for the chemical-mechanical polishing (CMP) damascene gate process. Nitride isolation, though not necessary, was chosen to avoid any over etch in later steps involving DHF. Fins were defined using deep ultraviolet lithography and dry etching processes (Fig. 2(a)). Gate oxide of 4.5nm was thermally grown in dry oxygen on the sidewalls of the channel followed by gate amorphous-silicon deposition using LPCVD process. CMP was used to planarize the surface, stopping on the silicon nitride hard mask and thus isolating both gates as can be seen in Fig. 2(b).

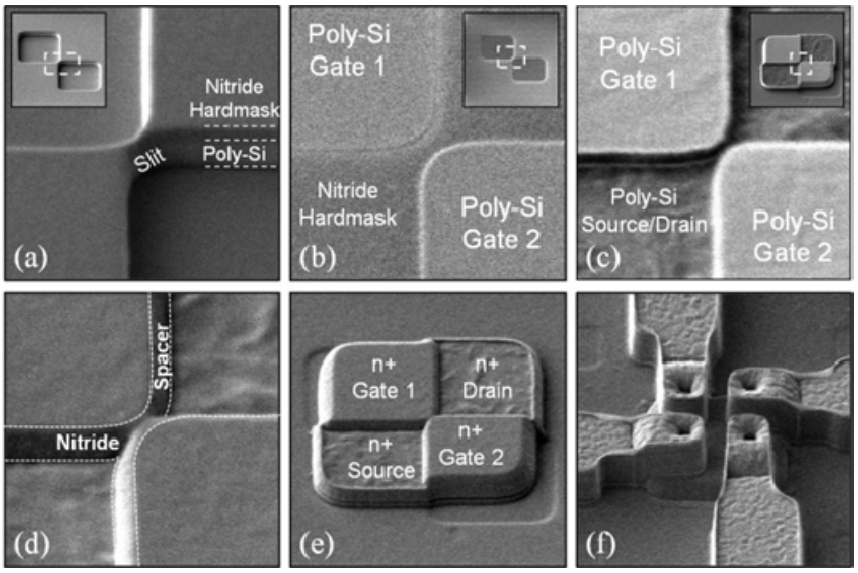

Fig. 2: Tilted view scanning electron micrographs after (a) nitride hard mask etch and poly-silicon fin/slit etch, (b) poly-Si gate CMP, (c) nitride hard mask wet etching to expose poly-silicon source/drain, (d) nitride spacer formation across slit, (e) source/drain/gate isolation formation, and (f) metallization with four terminals. Insets in (a)-(c) are low magnification images of the respective patterns.

The silicon nitride hard mask is subsequently removed by phosphoric acid wet etching, to yield a step between the higher poly-silicon gate and the lower poly-silicon source/drain surface, shown in Fig. 2(c). Silicon nitride (80nm) was subsequently deposited and etched to form a spacer surrounding the step of poly-silicon gate over active poly-silicon. The two spacers in the narrow opening between the two gates touch each other and thus cover the slit channel completely from the top as seen in Fig. 2(d). The wafer was then implanted with arsenic and activated to dope the gate and source/drain electrodes. The nitride spacer protected the channel from being doped (remained un-doped), thus defining the channel length independent of lithography, which is the novelty of this work. Next, formation of source/drain/gate isolation was achieved by active area patterning and etching, as shown in Fig. 2(e). Finally, a pre-metal dielectric oxide layer was deposited, followed by contact hole etching and standard metallization processes, shown in Fig. 2(f).

3. Results and Discussion

We characterized the fabricated devices using HP4156C parametric analyzer. Shown in Fig. 3(a) are the I_D-V_G plots in linear (V_D = 0.05V) and saturation (V_D = 1.2V) regions. Without any doping in the channel, device behaved as an inversion mode MOSFET with threshold voltage (V_T) ~ 0.8V. Subthreshold slope (SS) is 120mV/dec, which is very good considering poly-silicon channel. Drain induced barrier lowering (DIBL) of 150 mV/V indicates good electrostatic control of the gate on the channel. It is worth mentioning here that device has physical channel length of ~ 100 nm and is made from a single implant without lightly doped drain (LDD) thus electrical channel length is expected to be very small. The I_D-V_D characteristics of the device at different V_G values are shown in Fig. 3(b) showing slow saturation which indicates slightly high series resistance. Despite high series resistance, relatively high V_T, and poly silicon channel material, a drive current of 1.16 µA is obtained from a 0.11µm tall channel at an overdrive (V_G-V_T) = 0.4V, which is normalized to 10.55 µA/µm.

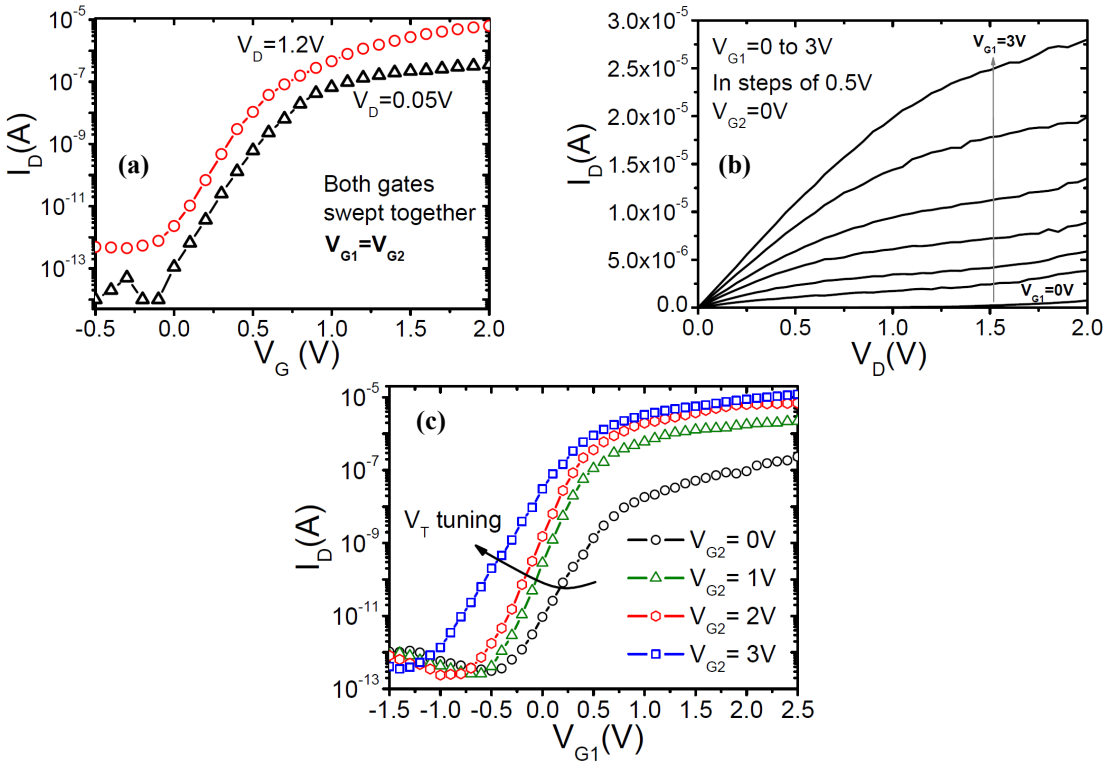

Fig. 3: (a) I_D-V_G and (b) I_D-V_D graphs of the fabricated device. (c) I_D-V_G in saturation region with one gate swept and other biased at a fixed potential.

Shown in Fig. 3(c) is the I_D-V_G in saturation region (V_D = 1.2V) with one gate swept and other biased at a fixed potential. The influence of one gate on the other is clearly observed. As a result of interaction

between the two gates and independent control of the gates, a V_T tunability range of ~1V is obtained for V_{G2} from 0 to 3V.

4. Conclusion

A novel method to fabricate independent double-gate FinFETs with self-aligned source/drain junctions was presented. The gates were defined using damascene process and pinch-off between the two spacers was utilized to define lithography free sub-100 nm channel length. The fabricated *n*-type thin film FinFETs demonstrated good electrical characteristics. The proposed integration scheme paves the way for future stacked circuit fabrication. The presented method can also be implemented on SOI or bulk silicon wafers for fabricating high performance devices.

5. References

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