

## Logic Functionality in Vertical Slit Field Effect Transistor (Vesfet)

Aashit Kamath<sup>1</sup>, Zhixian Chen<sup>1</sup>, Nansheng Shen<sup>1</sup>, Xiang Li<sup>1</sup>, Navab Singh<sup>1</sup>, Guo-Qiang Lo<sup>1</sup>, Dim-Lee Kwong<sup>1</sup>, Dominik Kasprowicz<sup>2</sup>, Andrzej Pfitzner<sup>2</sup> and Wojciech Maly<sup>3</sup>

<sup>1</sup> Institute of Microelectronics, A\*STAR (Agency for Science, Technology and Research), Singapore 117685

<sup>2</sup> Warsaw University of Technology, Poland

<sup>3</sup> Carnegie Mellon University

**Abstract.** This work follows the recent work on fabrication-based feasibility assessment of N-Channel Vertical Slit Field Effect Transistor (VeSFET) [1]. For the first time, we demonstrate AND/OR functionality in the single device by varying the slit width. The fabricated n-channel VeSFETs with AND and OR functionalities exhibit good electrical performance with low off current of  $10^{-13}$  A and high  $I_{ON}/I_{OFF}$  ratio of  $\sim 10^7$ .

**Keywords:** Vertical Slit Field Effect Transistors (VeSFET), junctionless device, multi-functionality, AND and OR logic functions, logic circuits

### 1. Introduction

Scaling of conventional planar MOS transistor is becoming increasingly challenging due to the increased short channel effects (SCE) in extremely scaled transistors. Multi-gate devices are being researched as a solution to SCE due to their enhanced gate control [2] with tri-gate MOSFET moving into manufacturing at 22 nm and below [3]. These devices can also offer more than just improved gate control, such as, increased function per transistor, provided, the gates are controlled separately [4]. Adding more functionality to a single device could be a way, other than scaling, to increase the functional density for a given silicon area. For example, realizing AND/OR functionality in a single transistor allows implementation of NAND logic with two transistors as compared to four in conventional CMOS based design. This could potentially lead to increased logic density per area. Furthermore, in a logic circuit, transistors connected in series (AND function) need to be of larger width to reduce the ON resistance, thus limiting the maximum number of inputs to a gate. By realizing AND functionality in a single transistor, every two transistors in series can be replaced with a single transistor, halving the series resistance and thus alleviating the problem of ON resistance [5].

While any independently controlled double gate transistors, such as 4T Fin-FET, can be used for implementing OR functionality, where the transistor is switched ON if any of the gates are biased 'High', implementing AND functionality is rather challenging. The junction-less Vertical Slit Field-Effect Transistor (VeSFET), proposed by Maly, *et al.* [6], shown in Fig. 1, is a suitable device architecture to implement both the AND and OR functions on the same device [7]. In addition to multi-functions, VeSFET offers many advantages, including no lithography on topography, and optical proximity correction (OPC) free device structure etc.

Following our recent work on fabrication-based feasibility assessment [1], in this report, for the first time, we experimentally demonstrate multi-functionality in the N-channel VeSFET by implementing AND and OR functions using slit width variation to switch functions. A device with wider slit width is used for OR function while narrower for AND. Both the devices demonstrate good electrical performance.

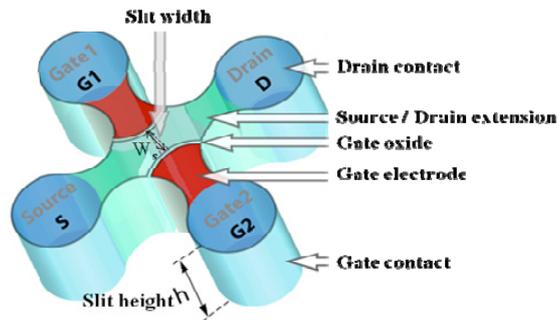


Fig. 1: Schematic drawing of junction-less VeSFET, with circularly-designed source/drain and gates that can be printed without complex OPC. The contact plugs to source /drain and gate can be through the top silicon to make the device vertically homogeneous and thus allowing interconnects from both sides

## 2. Device Operation Principle, Design And Implementation

A Junction-less VeSFET, shown schematically in Fig. 1, is a gated resistor in which the current is controlled by depletion regions created by the two gates on either side of the channel [1, 6]. In the OFF state, the depletion region, created due to the work function difference between the channel and the gate material, packs up the channel completely, leading to low OFF current. In the ON state, when a voltage is applied on the gate to counter the work function difference, the depletion region recedes and a path is created for the current to flow between source and drain. AND and OR functionality can be implemented in VeSFETs by controlling how the depletion regions created by the two gates overlap. There could be two ways to manipulate this overlap: (1) by using different doping level in the channel and (2) by using different slit width. The concept of using different doping level was recently published based on simulation results [7]. The variation of slit width has advantage in number of processing steps over different doping level and thus has been opted in this work.

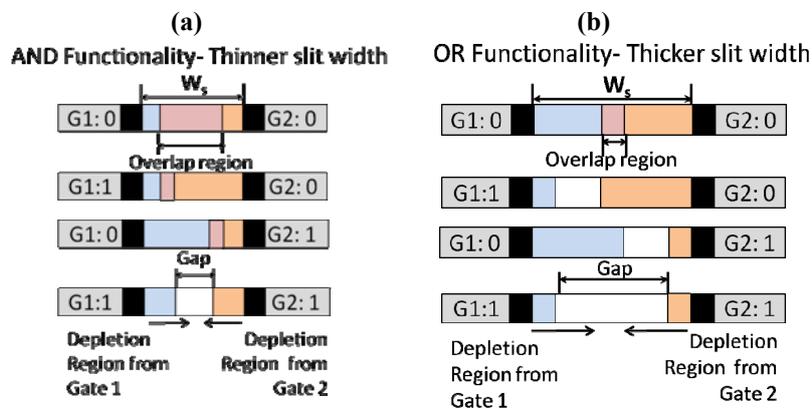


Fig. 2: Schematic illustration of switching functionality between AND and OR by varying the slit width controlling the overlap of the depletion regions. (a) AND functionality with large overlap in depletion region such that high potential on one of the gates is unable to open the channel and (b) OR functionality with small overlap of depletion where high potential on any of the gates can open the channel. The concept is analogous to sliding doors with overlap

The concept of AND and OR function implementation using slit width variation is illustrated schematically in Fig. 2. It is analogous to the sliding doors designed with overlap. In AND type transistors the depletion regions from gate-1, owing to smaller slit width, approaches gate-2 dielectric (spread over full channel) and vice versa. Thus, the overlap of the depletion region caused by the work function of two gates is almost across the entire channel width thus resulting in low current when both the gates are biased low, corresponding to an OFF state. When high voltage ( $V_{DD}$ ) is applied on one of the gates, the corresponding depletion region recede, however, the depletion region due to the other gate still blocks the channel, thus retaining the device in OFF state. However, when high voltage ( $V_{DD}$ ) is applied to both the gates, depletion

regions corresponding to both the gates recedes and creates a path for the current to flow, corresponding to an ON state, thus demonstrating an AND functionality.

In OR type transistors the depletion regions due to both the gates, owing to larger slit width, reach only till the middle of the channel with little overlap at the center. When high voltage ( $V_{DD}$ ) is applied to any one or both the gates, the corresponding depletion region recedes, creating a path at the center for the current to flow, giving the device an OR functionality.

We fabricated both AND and OR type transistors on a single 8" p-type boron doped ( $10^{15} \text{ cm}^{-3}$ ) SOI wafers with 117nm top silicon on 145nm bottom oxide (BOX) similar to [1]. Slit width obtained was 42 nm for AND type device and 88 nm for OR type device with a slit doping of  $5 \times 10^{17} \text{ cm}^{-3}$  (phosphorus) and gate doping of  $10^{21} \text{ cm}^{-3}$  (boron). Fig. 3 presents the final fabricated device and cross-sectional transmission electron micrograph (TEM) taken across the slit showing channel dimensions (corresponding to an OR type device) and the two independent gates.

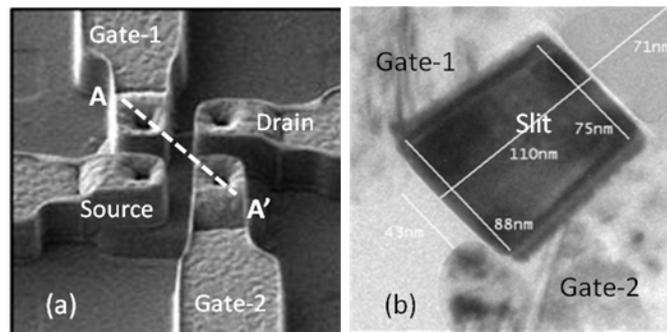


Fig. 3: (a) SEM image of final device and (b) cross-sectional TEM across the slit (A-A') showing the two independent gates for an OR device.

### 3. Results and Discussion

We characterized both the devices by applying different fixed potentials, corresponding to high or low state, on one gate and sweeping the other gate from low to high state to check AND and OR behavior. Fig. 4(a) shows the  $I_d-V_g$  of a typical OR type transistor. State '00' is when both the gates are biased at 0V. At this bias the device is in the OFF state as depletion region due to the work function difference between the gate and the channel material has filled up the complete channel. A low OFF current of  $4 \times 10^{-13} \text{ A}$  is measured. For state '10', '01' or '11', one or both the gates are biased at 1.2 V. Consequently, the corresponding depletion region recedes and thus turns the device ON state with an ON current of  $3 \times 10^{-6} \text{ A}$ .

Fig. 4(b) shows the  $I_d-V_g$  characteristics of a typical AND type transistor. State '00', '10' or '01' is when one or both the gates are biased at 0V. At this bias the device is in the OFF state as depletion region overlap is spread across the complete channel. Any one of the gates biased high is unable to turn on the transistor. A low OFF current of  $1.5 \times 10^{-13} \text{ A}$  is measured. For state '11' both the gates are biased at 1.2V. Consequently, the depletion regions recede and the device is in the ON state, and an ON current of  $6 \times 10^{-6} \text{ A}$  is measured.

Using AND and OR transistors in logic circuits results in significant area savings. For example, consider implementation of NAND gate using multifunctional VeSFETs where the pull up network (two PMOS in parallel) is replaced with a single p-channel OR VeSFET and the pull down network (two NMOS in series) with a single n-channel AND VeSFET. The VeSFET NAND gate occupies a  $32F^2$  area, which is 60% less in comparison to the  $81F^2$  occupied by conventional NAND gate, where F is half pitch or minimum feature size. It is also worth mentioning that the vertical homogeneity of VeSFET allows slit height tuning before interconnection through selective etching and thus matching n and p-performance can be without any area penalty.

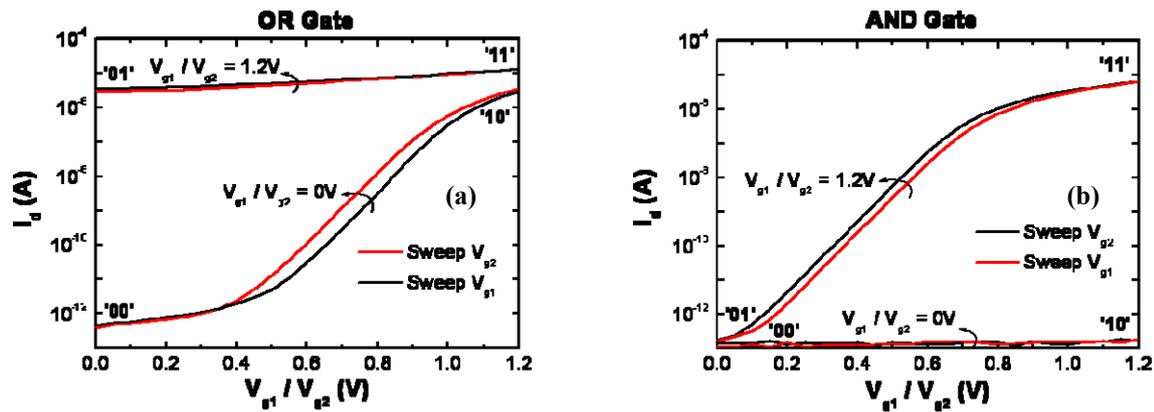


Fig. 3:  $I_d$ - $V_g$  curves of a typical (a) OR type and (b) AND type transistor.

## 4. Conclusion

Using the independent gate operation of the junctionless VeSFET, this paper demonstrated AND/OR functionality in a single transistor. Control of depletion regions overlap to switch functionalities was achieved using slit width variation. In addition to ease of fabrication of the device, 60% area saving in NAND logic make VeSFET based circuits promising candidate for ULSI.

## 5. References

- [1] W. Maly, A. Pfitzner, D. Kaspruwicz, W. Kuzmicz, N. Singh, Y-W. Lin, Z. Chen, N. Shen, X. Li, M. Marek-Sadowska. Twin Gate, Vertical Slit FET (VeSFET) for Highly Periodic Layout and 3D Integration. In: *IEEE MIXDES*. 2011, pp. 145-150.
- [2] J.-P. Colinge. *FinFETs and Other Multi-Gate Transistors*. SpringerLink, 2008, pp 1-48, DOI: 10.1007/978-0-387-71752-4\_1.
- [3] Intel Newsroom. *Intel 22nm 3-D Tri-Gate Transistor Technology*. Link: <http://newsroom.intel.com/docs/DOC-2032>.
- [4] M.-H. Chiang, K. Kim, C.-T. Chuang, C. Tretz. High-Density Reduced-Stack Logic Circuit Techniques Using Independent-Gate Controlled Double-Gate Devices. *IEEE Trans. On Electron Devive*. 2006, **53** (9): 2370-2377.
- [5] A. Datta, A. Goel, R. T. Cakici, H. Mahmoodi, D. Lekshmanan, K. Roy. Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices. *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*. 2007, **26** (11): 1957 - 1966.
- [6] W. Maly. Integrated Circuit Fabrication and Associated Methods, Devices and Systems. U.S. Non-Provisional Patent Application Serial Number CMU Docket 06-091; DMC Docket06-001PCTCMU.
- [7] M. Weis, R. Emling, D. S. Landsiedel. Circuit design with Independent Double Gate Transistors. *Advances in radio Science*. 2009, **7**: 231-236.