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Characterization of Variable Gate Oxide Thickness MOSFET with Non-Uniform Oxide Thicknesses for Sub-Threshold Leakage Current Reduction

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Abstract. As the technology scaling is entering the nanometer regime, the dominant problem which come into the scenario are, the increased short-channel effects (SCEs). Among the SCEs sub-threshold conduction is a very serious problem faced by the Semi-conductor industry. In the deep submicron regime, as the source and drain are closer to each other, the charge carriers diffuse through the region between source and drain in the static mode of operation of MOS (Metal Oxide Semiconductor) transistor circuits. In this paper, approaches at the device level, for reducing sub-threshold leakage current are addressed. Approaches of stacked gate materials in MOSFET are proposed and simulated. These simulations are carried out using Sentaurus TCAD (Technology Computer Aided Design). The simulations show a gradual decrease in the weak inversion current. Among the six devices simulated, there is a substantial reduction of sub-threshold current by 4.7μA and 6.2μA for two of the devices due to the topology of the gate and oxide stacks.

Keywords: Variable gate oxide thickness MOSFET (Metal Oxide Semiconductor Field Effect Transistor), gate oxide thickness, sub-threshold leakage current.

1. Introduction

As the technology is advancing into the deep sub micron regime, the demand for power-sensitive designs has grown significantly. This tremendous demand has mainly been due to the fast growth of battery-operated portable applications such as notebook and laptop computers, personal digital assistants, cellular phones, and other portable communication devices. Further, due to the aggressive scaling of transistor sizes for high-performance applications sub-threshold leakage current increase exponentially, this is considered as a very serious short channel effect [1].

A MOS transistor is called a short-channel device if its channel length is on the same order of magnitude as the depletion region thicknesses of the source and drain junctions. Alternatively, a MOSFET can be defined as a short-channel device if the effective channel length is approximately equal to the source and drain junction depth. In small geometry MOS transistors, the current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate to source bias voltage (V_{gs}) is not sufficient to invert the surface, i.e., $V_{gs} < V_{th}$ the carriers (electrons) in the channel face a potential barrier that blocks the flow [2],[3].

Increasing the gate voltage reduces this potential barrier and eventually allows the flow of carriers under the influence of the channel electric field. This simple picture becomes more complicated in small-geometry MOSFETs, because the potential barrier is controlled by both the gate-to-source voltage V_{gs} and the drain-to-source voltage V_{ds}. If the drain voltage is increased, the potential barrier in the channel decreases, leading to

drain-induced barrier lowering (DIBL) [4],[5]. The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage (V_{th}). The channel current that flows under these conditions ($V_{gs} < V_{th}$) is called the weak inversion current or sub-threshold current.

In MOS transistor digital circuits, the total power dissipation is divided into functional power and parasitical power and is given by equation (1). The functional power is the power required to just change the state capacitors charges of a digital circuit while processing the information i.e. in the active mode of operation of the circuit [6],[7].

$$P_{total} = P_{functional} + P_{parasitical} \quad (1)$$

The parasitical power is combination of leakage power and short-circuits power and is given by equation (2). The leakage power is the power which is dissipated and dominant when the circuit is idle. The short-circuit power is the power which could be dissipated during state transitions without attributing to the actual changes of the internal states [6],[7].

$$P_{parasitical} = P_{leakage} + P_{short\text{-}circuit} \quad (2)$$

Leakage power is combination of many other current components such as channel edge current, DIBL current and weak inversion current. The weak inversion currents increase exponentially under constant field scaling conditions due to down scaling of threshold voltage. Also the weak inversion current has an inverse dependency on gate oxide thickness. This can be clearly observed from the equation (3). As a result power dissipation caused by weak inversion current becomes dominant during standby periods, because functional and short-circuit power dissipation are non-existent during the standby periods [6],[7].

$$I_{sub} = \mu_0 \frac{\varepsilon_{ox}}{t_{ox}} \frac{W}{L} V_t^2 \left(e^{\frac{V_{gs} - V_{th} + \eta V_{ds}}{n V_t}} \right) \left(1 - e^{\frac{-V_{ds}}{V_t}} \right) \quad (3)$$

Where I_{sub} is the sub-threshold current, W and L are the width and length of the transistor, μ_0 is the carrier mobility, V_t is the thermal width, η is the DIBL coefficient, n is the sub-threshold swing, V_{ds} is the drain to source voltage, V_{gs} is the gate to source voltage, V_{th} is the threshold voltage, ε_{ox} is the permittivity of the oxide, t_{ox} is the thickness of the oxide.

A transistor level approach for reducing sub-threshold leakage current has been reported in [8]. In [8] thickness of the oxide has been varied uniformly. In this paper based on the I_{sub} and t_{ox} dependency relation, different gate structure topologies are proposed to study the effect of variation of I_{sub} for different non uniform t_{ox} combinations. All the possible combinations of the gate oxide thicknesses are considered and are shown in Fig.1a, Fig.2 to Fig. 6 respectively. Their V_{gs} vs I_d characteristics are shown from Fig.7 to Fig.12 respectively.

2. Variable gate oxide thickness MOSFET

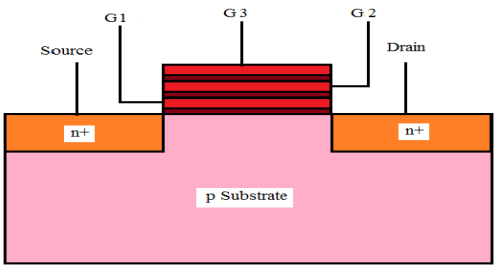


Fig. 1: Variable gate oxide thickness MOSFET

A variable gate oxide thickness MOSFET is shown in Fig.1. It consists of stacked gate structure. The gate terminals are named as G1, G2 and G3. When the MOSFET is biased, the weak inversion region is formed for the voltage $0 < V_{gs} < V_{th}$. In these conditions $I_d = I_{sub}$. When the gate G1 is considered, the operation is similar to a normal MOSFET, while the gate G2 terminal is considered the sub-threshold current is lowered to that of the current at G1 because the threshold voltage of the transistor is altered when the oxide thickness is increased. So the measured current is lower compared to the current measured at G1.

When the gate G3 terminal is considered for the operation of the MOSFET, the sub-threshold current is still low compared to the sub-threshold currents at G1 and G2 terminals. The threshold voltage of the transistor increases in this case because the oxide thickness has been increased. So only less current flows between source and drain.

3. Approach for non-uniform oxide thicknesses in Variable Gate oxide thickness MOSFET

In [8] thickness of the oxide has been varied uniformly. In this paper based on the I_{sub} and t_{ox} dependency relation, different gate structure topologies are considered to study the effect of variation of I_{sub} for different non uniform t_{ox} combinations.

For all the devices i.e. Device 1, Device 2, Device 3, Device 4, Device 5, and Device 6 which are shown in Fig.1a, Fig.2 to Fig.6 respectively, the thinner gate terminal thickness is $10A^0$ (A^0 is Angstrom unit which is one tenth of nano), thicker gate terminal thickness is $20A^0$ and the thickest gate terminal thickness is $30A^0$. The thickness of the oxide is $5A^0$. 110nm technology has been used for the simulations. The substrate is Silicon material, gate is poly crystalline silicon and the oxide is silicon dioxide (SiO_2). The gate structures, V_{gs} vs I_d characteristics and the sub-threshold leakage current (I_{sub}) values are shown in the following table.

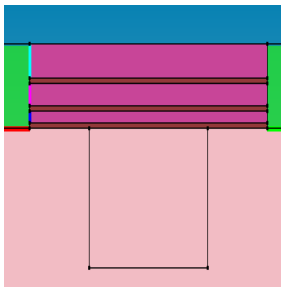
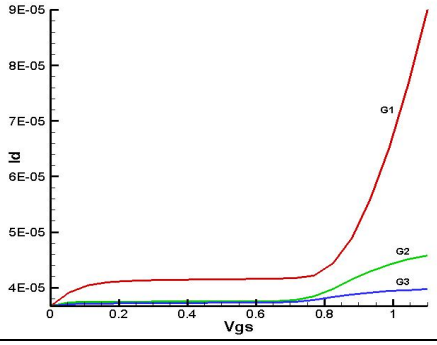
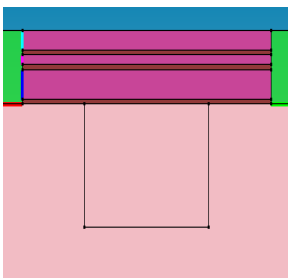
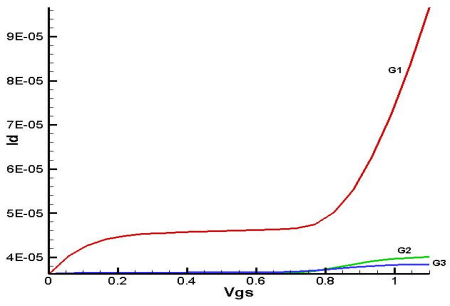
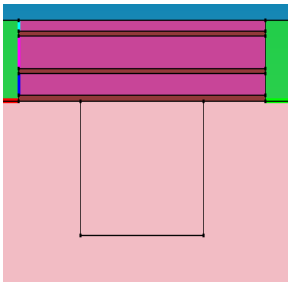
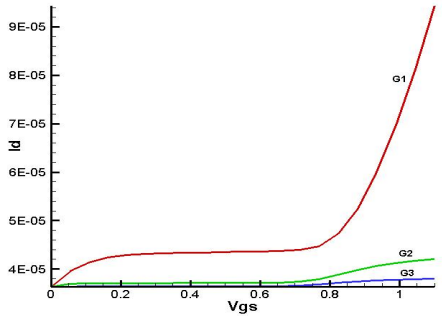
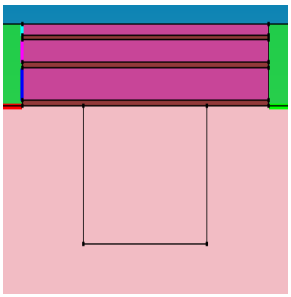
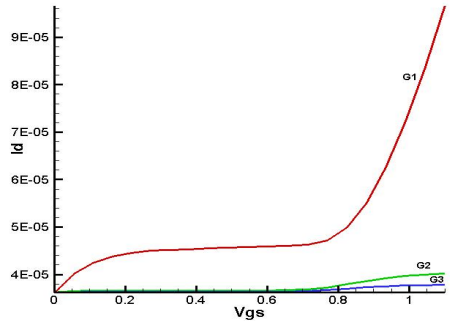
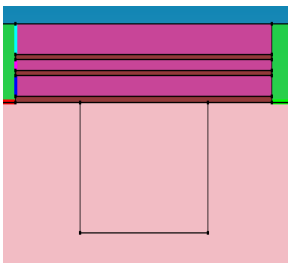
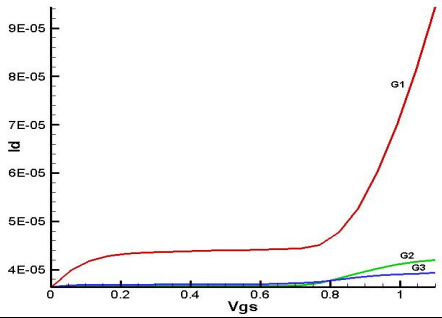
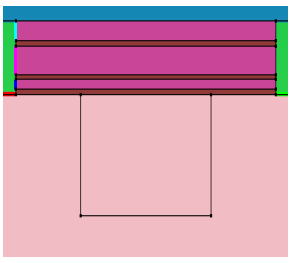
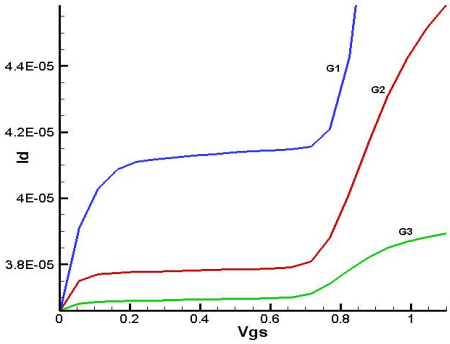
Device Gate structure	**V_{gs} vs I_d Characteristics**	**Gate terminal**	**I_{sub} (µA)**
Fig.1a :Device 1 	Fig.7 : Device 1 characteristics 	G1	39.5
		G2	37.8
		G3	37.4
Fig.2 :Device 2 	Fig.8 : Device 2 characteristics 	G1	45
		G2	40.2
		G3	39

Fig.3 :Device 3 	Fig.9 : Device 3 characteristics 	G1	42
		G2	37.8
		G3	37.3
Fig.4 :Device 4 	Fig.10 : Device 4 characteristics 	G1	45
		G2	40
		G3	38.8
Fig.5 :Device 5 	Fig.11 : Device 5 characteristics 	G1	42
		G2	40
		G3	38.8
Fig.6 :Device 6 	Fig.12 : Device 6 characteristics 	G1	39.5
		G2	38.7
		G3	37.3

4. Implementation and results

The gate structure of Device 1 shown in Fig.1a is the combination of three gate over gate structures whose lower gate terminal thickness is $10A^0$, middle gate thickness is $20A^0$ and the top gate thickness is $30A^0$. If the below terminal i.e. gate G1 is considered for biasing the thickness of the oxide seen is $5A^0$. If the middle terminal i.e. gate G2 is considered for biasing, the effective oxide thickness seen is combination of the thicknesses of the bottom oxide layer, thickness of gate G1 and thickness of the middle oxide layer. This effective thickness is considered to be the total thickness of the oxide at this terminal. Hence the total oxide thickness observed at gate G2 is $20A^0$. Now if the top terminal i.e. gate G3 is considered for biasing, the effective oxide thickness seen is combination of the thicknesses of the bottom oxide layer, thickness of gate

G1, thickness of the middle oxide layer, thickness of gate G2 and thickness of the top oxide layer. Hence the total oxide thickness observed at gate G3 is $45A^0$. The sub-threshold currents measured from the V_{gs} vs I_d characteristics shown in Fig.7 for the individual biasing of gates G1, G2 and G3 of Device 1 are 39.5 μA, 37.8 μA, 37.4 μA respectively.

The gate structure of Device 2 is shown in Fig.2. The lower gate terminal thickness is $30A^0$, middle gate thickness is $10A^0$ and the top gate thickness is $20A^0$. If the below terminal i.e. gate G1 is considered for biasing the thickness of the oxide seen is $5A^0$. If the middle terminal i.e. gate G2 is considered for biasing, the effective oxide thickness seen is combination of the thicknesses of the bottom oxide layer, thickness of gate G1 and thickness of the middle oxide layer. This effective thickness is considered to be the total thickness of the oxide at this terminal. Hence the total oxide thickness observed at gate G2 is $40A^0$. Now if the top terminal i.e. gate G3 is considered for biasing, the effective oxide thickness seen is combination of the thicknesses of the bottom oxide layer, thickness of gate G1, thickness of the middle oxide layer, thickness of gate G2 and thickness of the top oxide layer. Hence the total oxide thickness observed at gate G3 is $55A^0$. The sub-threshold currents measured from the V_{gs} vs I_d characteristics shown in Fig.8 for the individual biasing of gates G1, G2 and G3 of Device 2 are 45 μA, 40.2 μA, 39 μA respectively.

The gate structure of Device 3 is shown in Fig.3. The lower gate terminal thickness is $20A^0$, middle gate thickness is $30A^0$ and the top gate thickness is $10A^0$. If the below terminal i.e. gate G1 is considered for biasing the thickness of the oxide seen is $5A^0$. If the middle terminal i.e. gate G2 is considered for biasing, the effective oxide thickness seen is combination of the thicknesses of the bottom oxide layer, thickness of gate G1 and thickness of the middle oxide layer. This effective thickness is considered to be the total thickness of the oxide at this terminal. Hence the total oxide thickness observed at gate G2 is $30A^0$. Now if the top terminal i.e. gate G3 is considered for biasing, the effective oxide thickness seen is combination of the thicknesses of the bottom oxide layer, thickness of gate G1, thickness of the middle oxide layer, thickness of gate G2 and thickness of the top oxide layer. Hence the total oxide thickness observed at gate G3 is $65A^0$. The sub-threshold currents measured from the V_{gs} vs I_d characteristics shown in Fig.9 for the individual biasing of gates G1, G2 and G3 of Device 3 are 42 μA, 37.8 μA, 36.2 μA respectively.

Similar analysis is done for Device 4, Device 5 and Device 6 which are shown in figures Fig.4, Fig.5 and Fig.6 respectively. The V_{gs} vs I_d characteristics of the MOSFETs Device 4, Device 5 and Device 6 are shown in figures Fig.10, Fig.11 and Fig.12 respectively. The sub-threshold currents measured for the Device 4 at the three gate terminals G1, G2 and G3 are 45 μA, 40 μA, 38.8 μA respectively. The sub-threshold currents measured for the Device 5 at the three gate terminals G1, G2 and G3 are 42 μA, 40 μA, 38.8 μA respectively. The sub-threshold currents measured for the Device 6 at the three gate terminals G1, G2 and G3 are 39.5 μA, 38.7 μA, 37.3 μA respectively.

5. Conclusion

For devices like mobile phones, remote controllers which have more standby operation than the active mode of operation, Device 4 like structures can be used as the sleep transistors in the non critical paths of the circuit, because the comparative sub-threshold leakage current measured for this device is very low in comparison to the sub-threshold leakage currents measured for the other devices. Therefore this kind of device ensures longer battery time.

For applications like computer monitors which have semi standby mode of operation for more instances of the time, Device 3 like structures can be used because the sub-threshold leakage currents measured for this device are very marginal in comparison to the sub-threshold leakage currents measured for the other devices. Therefore this kind of device ensures quick response for any interrupt.

Although each and every device simulated has their own advantages and disadvantages, the usage of them depends on the user's application and the mode of operation of the electronic gadget.

6. References

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