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A 1.5-V Wideband, Noise-Cancelling LNA in 0.13um CMOS

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Abstract: The first step to implement the software radio is to achieve a linear, wide-band low noise amplifier (LNA). A noise-cancelling wideband LNA in 0.13um CMOS technology is presented in this paper. The LNA consists of a common gate input stage with the broadband input matching network design, and a following common source auxiliary stage for the noise and distortion cancellation. The LNA can achieve a 600MHz-6GHz bandwidth, a nominal gain of 17dB, a minimum noise figure of 2.3dB, a maximum IIP3 of 4dBm using a 130nm RF CMOS process, and consumes 12mW from a 1.5-V supply.

Keywords: noise-cancelling, low-noise amplifier, broadband match, radio frequency integrated circuit.

1. Introduction

Multi-band wireless communication system has been investigated. The software radio [1], a programmable device that severs multiple bands and modes, can cover all major commercial communication bands up to 6GHz. As a result, the RF front-end should cover every communication standard, including providing relatively uniform gain and an input impedance close to 50-Ohm within that frequency range, while handing the full dynamic range of the wideband spectrum incident on the antenna, without significant distortion or noise corrupting desired signals. The first step towards a multi-band front-end is a linear, wide-band low noise amplifier (LNA).

Design of a tuneable or wideband front-end amplifier has many benefits compared to parallel narrowband receiving paths. It can provide better reconfigurations as well as greater area and power efficiency. The distribution approach [2] and resistive feedback method [3][4], transformer-based feedback[5], active feedback[6], and multiple parallel feedback loops [7], have been used to design conventional wideband amplifiers. However, the distributed approach often suffers from high power consumption and low gain, while noise figure of resistive feedback is usually not good enough.

The use of wideband filtering and matching networks [8][9] is a good way to match the input impedance of the inductively degenerated LNA across a wide band. Also, in recently years, a noise-cancelling technique has become a promising technique in realizing wideband LNAs [10][11][12][13][15]. Another benefit of Noise-cancelling LNAs is that in principle it can achieve high linearity because the amplifier topology is capable of cancelling the distortion due to the matching element.

In this paper, a noise-cancelling wideband LNA is designed with a low-Q resonant input-matching network to provide high gain (17 dB), low noise figure (~3dB) and good input impedance match(S11<-10dB) over a wide frequency range (600M~6GHz) in 0.13um CMOS technology.

2. Noise Cancelling LNA

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The noise cancelling architecture used in this paper is shown in Fig.1(a). The common gate amplifier in the left branch sets the input impedance match, and the gain. The common source amplifier in the right branch is used to cancel the noise and distortion due to the fact that the noise of M1 and M2 appears as common-mode at differential output, as shown in Fig.1(b). The cascade transistors are added to improve reverse isolation.

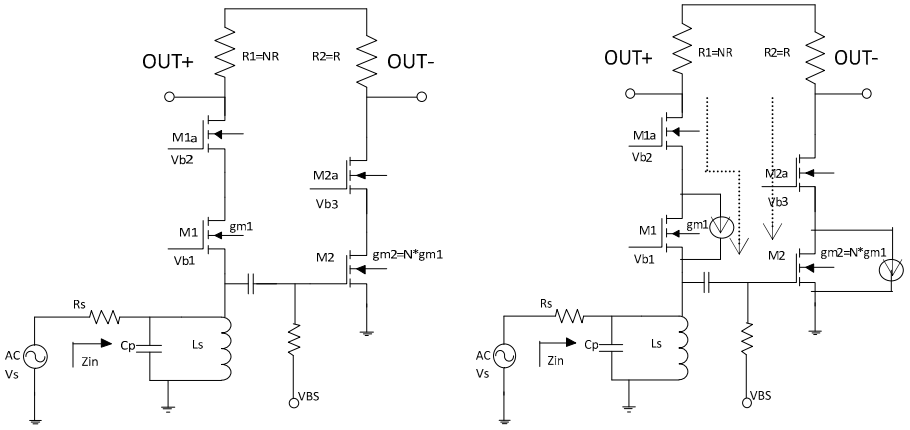


Fig.1(a) Single-to differential LNA (b) common mode noise in differential output

As it is well known, the common gate (CG) LNA present a broadband resistive input impedance and a noise factor usually larger than 3dB for short channel MOSFET device. By using the noise cancelling structure, the minimum noise figure is no longer dependent on the quality of its input power match, and both the optimization of power match and noise figure can be achieved.

2.1. Voltage Gain

The maximum voltage gains of the individual CG and CS stages are

$$A_{v,\,cg} \mid \max = g_{m1}(R1) \tag{1}$$

$$A_{v,\,cs} \mid \max = -g_{m2} * R2$$

And the maximum total LNA voltage gain is $A_{v,\,cg} \mid \max - A_{v,\,cs} \mid \max$

$$Av \mid \max = g_{m1} * R1 + g_{m2} * R2 \tag{2}$$

The transconductance of the common-gate devices M1 directly determines the LNA's input resistance, Rin=1/Gm1. With a single-ended input resistance of 50ohm required to provide a perfect input power match, the required M1 transconductance gm1 is 20ms.

2.2. Noise Figure

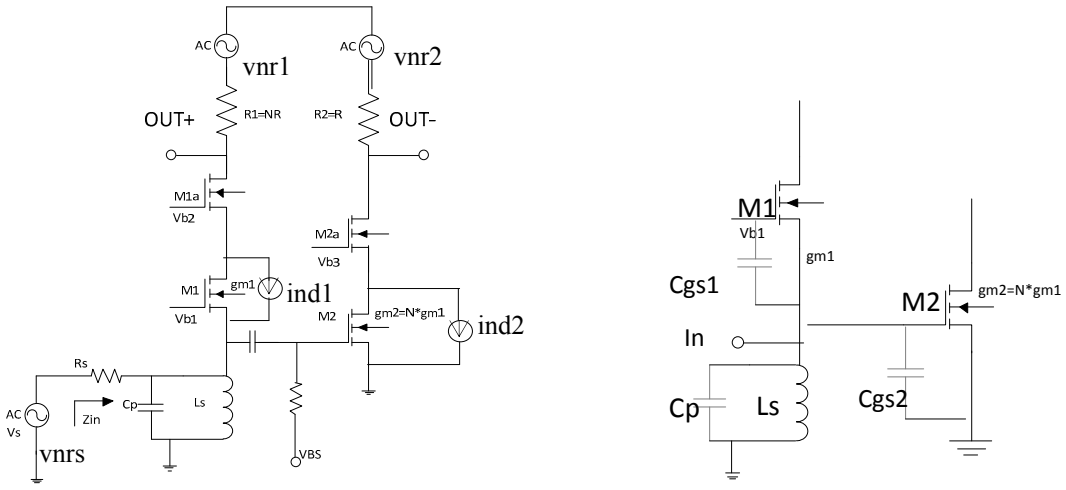


Fig2 (a) noise source of the circuit (b) Input Loading on the LNA under small signal operation

The primary sources of the noise in circuit of this topology are the drain current noises from both M1 and M2, the thermal noise from the total effective CG and CS stage load resistance, R1, R2, and the source resistance at the input, Rs[14],as shown in Fig2.(a). It is assumed that the cascade devices circulate their own noise currents and don't contribute any extra noise to the system. This is a reasonable assumption as long as $g_{m1a} << 1/r_{o1}$ and $g_{m2a} << 1/r_{o2}$, which forces all drain noise currents introduced by the cascades to flow back into their source terminals instead of through the M1 and M2 devices. The mean square output noise voltages due to each of the noise source presented in are given by (3):

$$\begin{aligned}
\overline{V_{no,d1}^2} &= 4KT\frac{\gamma_1}{\alpha_1}g_{m1}*\left(\frac{R_1 - Rs*g_{m2}*R_2}{1+g_{m1}*Rs}\right)^2\Delta f \\
\overline{V_{no,d2}^2} &= 4KT\frac{\gamma 2}{\alpha 2}g_{m2}*(R_2)^2\Delta f \\
\overline{V_{no,r1}^2} &= 4KTR_1\Delta f \\
\overline{V_{no,r2}^2} &= 4KTR_2\Delta f \\
\overline{V_{no,rs}^2} &= 4KTRs*\left(\frac{Av}{1+g_{m1}*Rs}\right)^2\Delta f
\end{aligned} \tag{3}$$

These output noise voltage expressions can be combined to calculate the system's noise factor across the matching bandwidth, as given in (4), where $\gamma = \gamma_1/\alpha_1 = \gamma_2/\alpha_2$.

$$F = 1 + \frac{\gamma(g_{m1}R_1 - g_{m2}R_2)^2}{Av^2} + \frac{4\gamma g_{m2}R_2^2}{Av^2}/Rs + \frac{4(R1+R2)}{Av^2}/Rs \tag{4}$$

The second item is due to the noise of M1 and M2. As you can see, if $g_{m1}R1 = g_{m2}*R2$, M1's noise contribution is zero. The drain noise from M1 is completely cancelled and the M1 term drops out of the noise factor expression. The third item is another part of noise introduced by the M2, the last item is due to load resistor noise. It is seen that the noise factor can be further lowered by adjusting g_{m2} and increasing *Av*.

2.3 Low-Q Resonant Input Matching Network

A resonant network exists at the input of the LNA with these inductors and the device capacitance, Fig.2(b) illustrates the various source of loading on the input nodes during small-signal operation. Here, C_{gs1} and C_{gs2} represent the gate-to-source capacitance of the sets of M_1 and M_2 devices, respectively. All other parasitic capacitances on each input node have been lumped together as a single C_p tied to ground. A small-signal input resistance is also presented by the CG devices to provide a good power match with the source resistance (50 ohm).The total capacitor seen in the input is given by (5)

$$C_{in} = C_{gs1} + C_{gs2} + C_p \tag{5}$$

Using this, the single-ended input impedance of the LNA can be expressed as (6)

$$Z_{in}(jw) = \frac{R_{in}}{1 + jR_{in}(wC_{in} - 1/wLs)} \tag{6}$$

Where R_{in} represents the small signal input resistance presented by the CG device. At resonance this network becomes purely resistive, and the LNA's input resistance is dominated by the small signal source resistance of the CG device, which should be designed to match the source resistance Rs. Keeping the LNA's input return loss(S11) below -10dB will maintain a good power match at the input of the LNA(less than 10% of incident power is reflected). The input matching bandwidth consists of the frequencies at which S11 is below -10dB: from $f_{s11,l}$ to $f_{s11,h}$. Ideally, for an SDR receiver, a broadband power match should be achieved over all common wireless standards from 600MHz up to 6GHz. Using (6), an expression for S11 can be calculated as S11 by (7)

$$S11 = 20\log\left|\frac{R_s^2(wC_{in} - 1/wL_s)}{\sqrt{(2R_s)^2 + (R_s^2(wC_{in} - 1/wL_s)^2)}}\right| \tag{7}$$

With the constrains of S11<-10dB, $f_{s11,l}$ to $f_{s11,h}$ is from 600MHz up to 6GHz, Rs=50ohm, we can pick up the Ls and Cin to meet this broadband match requirement.

2.4. Linearity

Noise cancelling topology can in principle achieve high linearity because the amplifier topology is capable of cancelling the distortion due to the matching element [15]. The mechanism behind this distortion cancellation is identical to that of the noise-cancellation. Undesired nonlinear small-signal current components introduced by the input matching device destructive interfere simultaneously along with its thermal drain current noise components. But it is critical to make sure that the noise and distortions added by the auxiliary amplifier are not larger than it is going to cancel. Ensuring this, however, often comes with higher power consumptions. Although, the cascade architecture is used in this paper, where the additional amplifying stages degrade linearity, the designed LNA can still get decent linearity (IIP3~4 dBm).

3. Implementation and Result

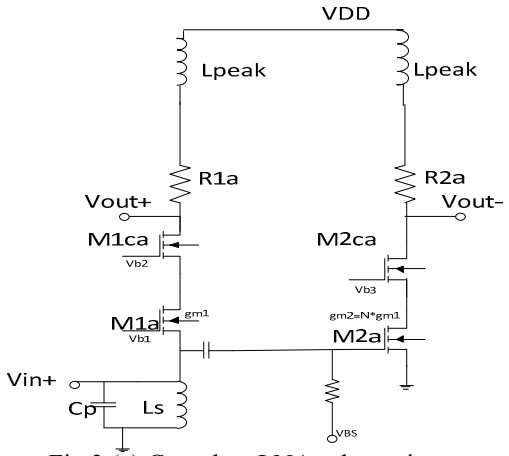
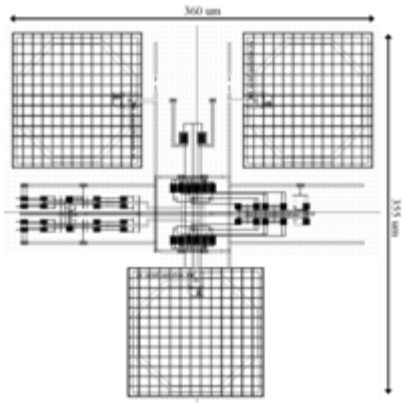


Fig.3 (a) Complete LNA schematic



(b) LNA core layout

A single-ended-to-differential LNA is implemented as show in Fig.3(a). The LNA is designed by combining the wideband input stage with wideband load to continuously cover a broad band application. The circuit was taped out using IBM 0.13um 8RF CMOS technology. Since the chip has not come back, data from simulation with layout parasitic are presented. The LNA core layout is presented in Fig.3(b).The core LNA size is 360umX355um including the bias circuit. The final design achieved the full 600MHz-6GHz bandwidth, a nominal voltage gain of more than 17dB as shown in the Fig.4(a) due to the wideband load used in the design. The S11 of the LNA is less than -10dB from 600MHz to 6GHz, with the lowest point around -46dB near 18GHz, due to the broad band match design in the input port.

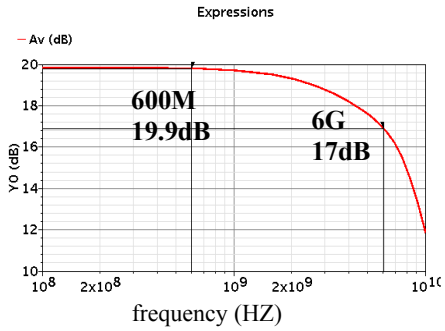
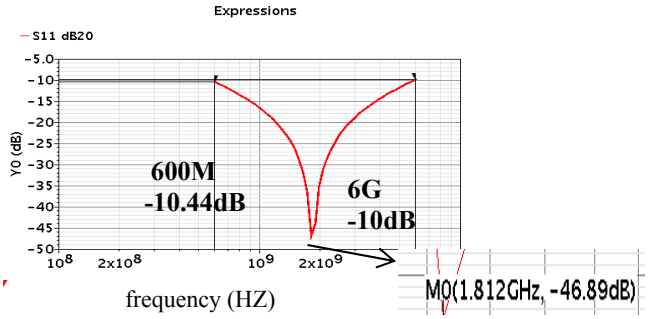
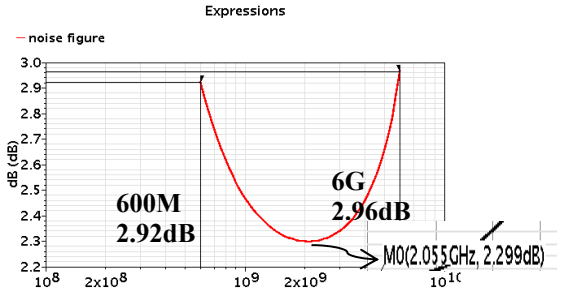


Fig.4 (a) The gain of LNA



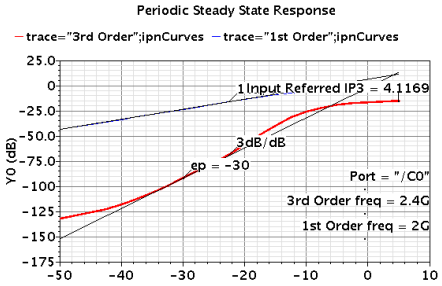
(b) The S11 of LNA

We can get a noise figure that ranged less than 3dB across the operating wide bandwidth, with 2.3dB around 2 GHz as shown in the Fig.5(a), due to the noise cancel architecture we use in this design. This noise cancel architecture also helps to get decent linearity as shown in the Fig.5 (b).



frequency (HZ)

Fig.5(a) The noise figure of LNA



Input Power (dBm)

(b) The IIP3 of LNA

Two sinusoidal tones located at 2/2.2 GHz model the strong desirable signal and on-chip transmitter leakage. They result in an IM3 product at 2.4GHz, which falls in the receiver band. As shown in Fig.5(b), The IIP3 is around 4dBm.The better IIP3 can be achieved with higher overdrive voltage($Veff = Vgs - Vt$), but that will consume more power. This performance was achieved with an overall power consumption of 12 mW with 1.5 supply.Table.1 summarizes the performance of the LNA along with results from recently published papers

Table I Performance Summary of Published CMOS Noise-Cancelling LNAs

	Technology [nm]	Frequency [GHz]	Gain [dB]	NF [dB]	IIP3 [dBm]	Power [mW]
[3]	180	3.1-5	5-10	2.3-5	-7	12.6
[10]	130	0.8-2.1	8-14.5	2.5-2.75	16	17.4
[15]	250	0-1.8	10-13.7	1.9-2.4	0	35
[11]	180	1.2-11.9	7.5-9.7	4.5-5.1	-6.2	20
[12]	0.09	2.5-4.0	17-19	4.0-5.4	-8	8
This Paper	130	0.6-6.0	17-20	2.3-3	4.0	12

4 Conclusion

This paper proposes a novel low noise, wideband impedance matched amplifier. It characterises its wideband impedance match of the common gate stage, and the low noise figure by cancellation. The 17dB LNA and 3dB noise figure from 600MHz to 6GHz gets from this Low noise amplifier, which is implemented in a 0.13um CMOS process.

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