2012 International Conference on Solid-State and Integrated Circuit (ICSIC 2012)
IPCSIT vol. 32 (2012) © (2012) IACSIT Press, Singapore

A Low Power 2 GHz Unity Gain Frequency with 154 PSRR CMOS OTA

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Abstract. In this paper a novel high frequency CMOS op-amplifier is proposed based on 0.18 μ CMOS technology. The proposed OP-Amp allows us to work not only at low voltage but also at high frequencies. The op-amp provides 39dB CMRR and 1.41 V/μs slew rate with 65º phase margin. To provide better performance a current buffer based compensate technique is used. As compared to conventional op-amp the proposed amplifier provides higher unity gain frequency. The proposed amplifier is simulated on electronics workbench and shows close agreement with theoretical approach.

Keywords: Op-Amp; 0.18μ CMOS Technology; Higher Unity Gain Frequency; Current Buffer Compensation; Operational Trans-Conductance Amplifier (OTA).

1. Introduction

In recent years, the importance of integrated circuits design with low supply voltage is increased. The operational amplifier (op-amp) which is a fundamental building block in the analog and mixed- mode circuits, is not an exception [1]. Some reasons can be given for the need to low voltage circuits [2]. First, as the integrated devices dimensions become smaller, gate-oxide with several nanometers thickness is subjected to lower breakdown voltages, so it requires lower supply voltage for ensuring device reliability. The second reason is due to increasing the demand of battery-powered portable equipment. In the portable device such as laptop, implantable cardiac pacemakers, wireless communication devices and hearing aids, low power dissipation is important to have suitable battery life and weight. In these applications, the supply voltage has to be reduced in order to have reasonable operation period from a battery. The third reason is dictated by increasing packaging density of the components on silicon chip. The chip can dissipate limited amount of power per unit area, hence power per electronic function has to be reduced in order to prevent overheating of the silicon chip. Ideally they perform the function of a voltage controlled current source, with an infinite voltage gain. Operational amplifiers are an integral part of many analog and mixed-signal systems. OPAMPs with vastly different levels of complexity are used to comprehend functions ranging from dc bias generation to high-speed amplification or filtering.

The design of OPAMPs continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies [3]. The realization of a CMOS OPAMP that combines a considerable dc gain with high unity gain frequency has been a difficult problem. There have been several circuit approaches to evade this problem. The simulation results have been obtained by NI Electronics Workbench &verified using S-edit and W-edit.

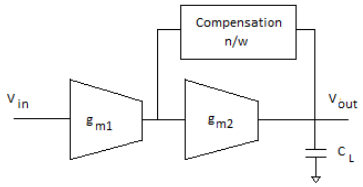

Fig. 1: Miller compensated two stages Op-Amp.

2. PROPOSED DESIGN

2.1 Circuit Description

The proposed designs consist of a differential pair amplifier for the purpose of high noise immunity as an input stage for output stage a common source amplifier is usedfor high gain, a current mirror circuit free from voltage sources as a biasing circuit, and a current buffer compensation circuit [7] is coupled with a Miller capacitance in series with one another [15].

Transistors Q1 and Q2 (NMOS) form the basic input stage of the amplifier. The gate of Q1 acts as an inverting input and the gate of Q2 as non-inverting input. The trans-conductance of this stage is the trans-conductance of Q1 or Q2. Q3 and Q4 behave as the active load transistors of the differential amplifier[14]. The utilization of current mirror as an active load gives following benefit to the circuit. [11][12][5][4]

- It provides a large output resistance in a relatively small die area.
- The current mirror topology performs the differential to single-ended conversion of the input signal and thus the load provides additional advantage to the CMRR.

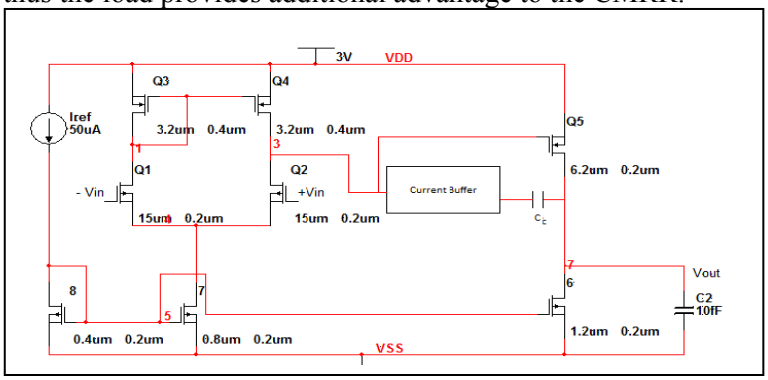

Figure 2. The Proposed Circuit

The common source amplifier (Q5) amplifies the output of the differential amplifier, Q1 and Q2 taking out from the drain of Q2 with the help of Q6 which acts as an active load for Q5 and provides additional gain to the circuit. The trans-conductance of this stage is approximately given by the trans-conductance of Q6. For appropriate mode of operation and for stabilization of desired Q-point transistor Q6, Q7, Q8 and current source (I_{ref}) provides biasing to the proposed circuit.

- Transistor Q8 and I_{ref}biased the Q7 and Q6 by providing appropriate voltage between their source and gate.
- Transistor Q6 and Q7 suppressed certain current which is proportional to the applied voltage (gate to source).
- Transistor Q8 must be operating in the saturation region and to ensure that a diode can be used.
- As transistor Q5 acts as an active load for current mirror it is automatically biased by gate to source voltage provided by current mirror.

The small signal gain of the differential amplifier is given by:

$$A_1 = g_{m1}(r_{01} \parallel r_{02})$$

Where g_{m1} is the trans-conductance of first stage.

The tangent K of the phase margin is

$$k = \tan\phi = W_{p2}/W_{GBW} \ldots..(1)$$

Where W_{GBW} = Gain Bandwidth Product

Ø= phase margin

W_{p2} = ratio of second pole (right hand plane)

It is also seen that W_{GBW} depends on the trans-conductance of the first stage, g_{m1} and on the compensation capacitance C_C and is related by the equation-

$$W_{GBW} = \frac{g_{m1}}{C_c} \qquad (2)$$

Where C_c is compensation capacitor.

2.2 Current Buffer Circuit

The primary use of current buffer circuit is to enhance the operating frequency. The compensation technique of current buffer approach uses a current buffer to break the forward path through compensation branch [4]. Considering an ideal current buffer in the compensation branch in place of the nulling resistor, the second pole frequency [5], [6] is-

$$W_{p2} = \frac{g_{m2}}{C_L\left(1 + \frac{C_{01}}{C_c}\right)}$$

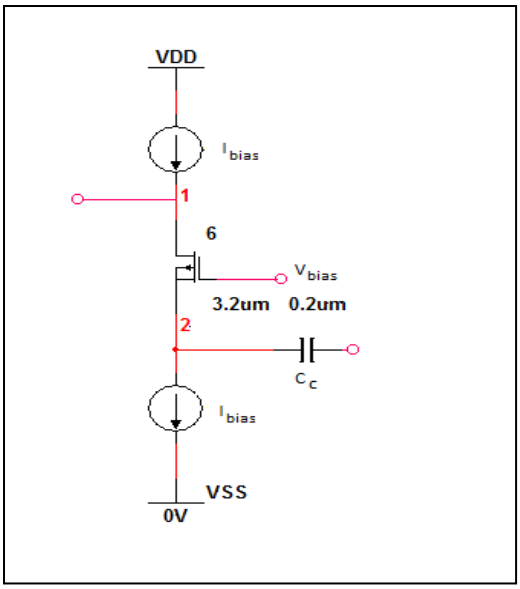

Figure 3. Current Buffer Compensation Circuit

This leads to a compensation capacitor [5] and can be expressed as-

$$C_c = \left(\frac{g_{m1}}{2g_{m2}}\right)KC_{01} + \sqrt{\left(\frac{g_{m1}}{g_{m2}}\right)KC_{01}C_L}$$

Where C_L is load capacitance

C_{01} = equivalent capacitance on the output of the first stage.

Substituting equation 2 and 3 in 1 and by solving approximately …

$$C_c = \left(\frac{g_{m1}}{2g_{m2}}\right) KC_L$$

3. Simulation Result

The proposed op-amp circuit simulated with a power supply of 3V and a load of 10fF. An AC signal of IV is applied with 5 points per decade in a frequency range of 10 KHz to 4 GHz for the frequency response plot.

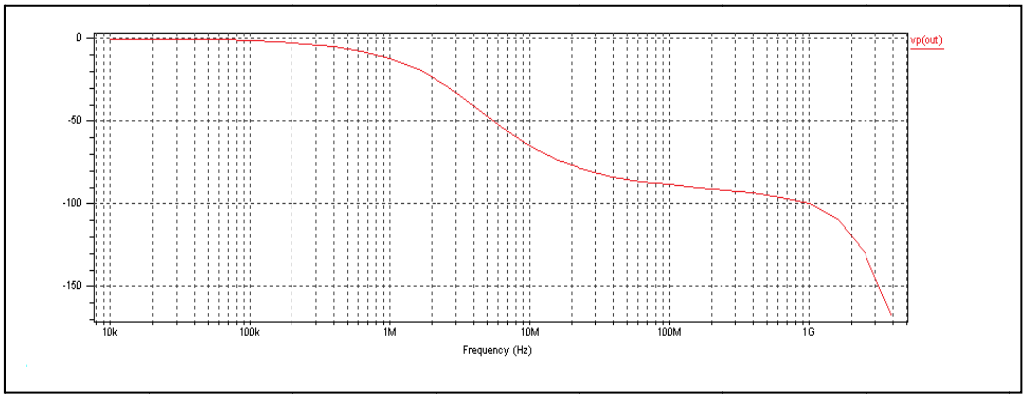

Figure 4a. Frequency response, Voltage phase (degree) vs. Frequency (Hz)

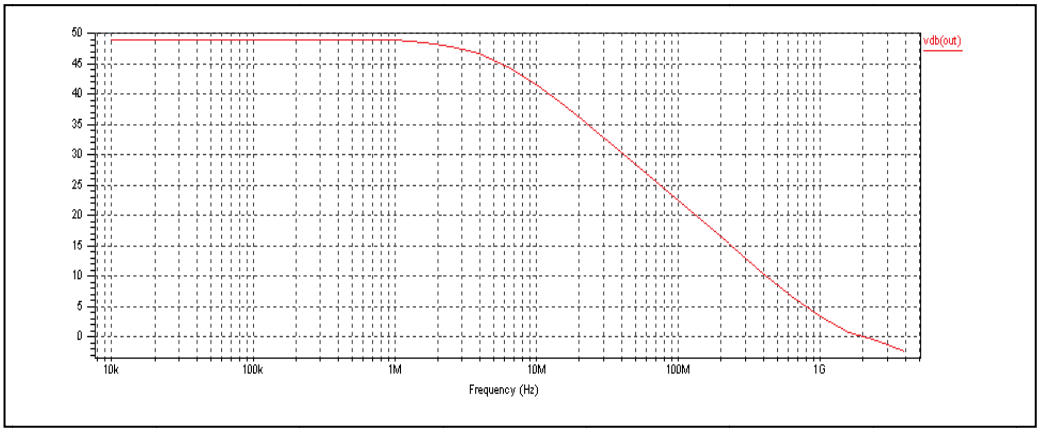

Figure 4b. Frequency response, Voltage magnitude (dB) vs. Frequency (Hz)

The simulation results shows that proposed circuit gives 49.05 dB DC gain and approx 61.2º, hence op-amp can be used for high speed operation (high frequency). The simulation result also suggested that proposed circuit possess a unity gain frequency of 2.05 GHz.

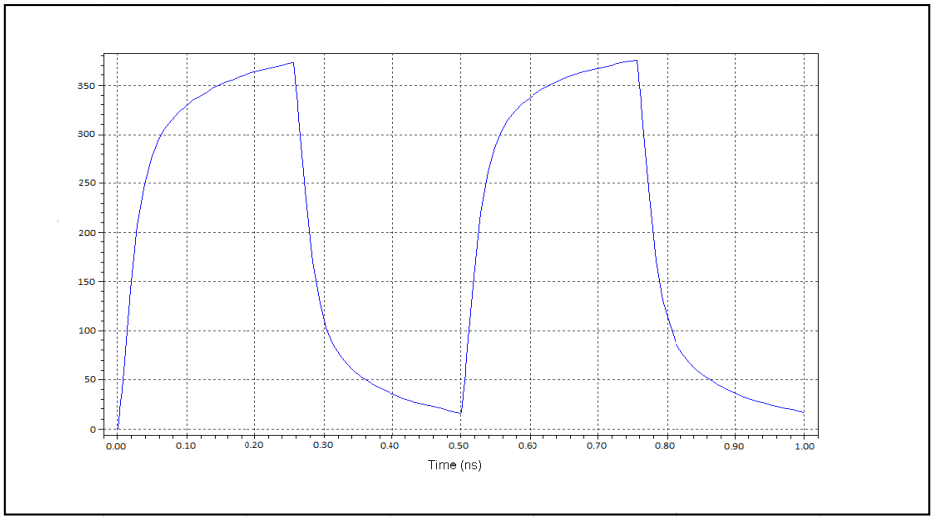

Figure 5. Slew Rate, Voltage (µV) vs. Time (ns).

Figure 5 shows the transient response of proposed op-amp, for simulation a 1mV pulse is applied with 0.5 ns pulse period[18], which gives slew rate of approx 1.41 V/µs (+ve& -ve).

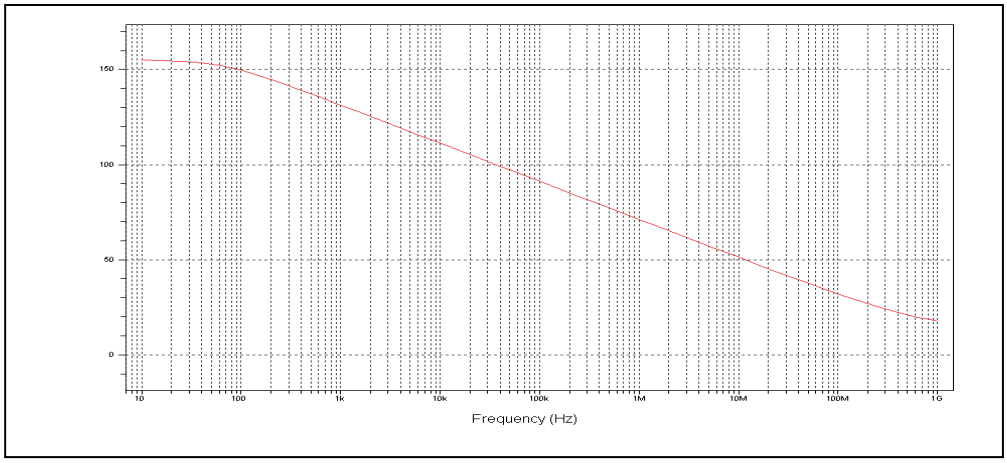

Figure 6. PSRR (dB) vs. Frequency (Hz)

Figure 6 shows simulation result of short input when op-amp is in unity gain configuration, or simply Power Supply Rejection Ration in dB. The calculative +ve PSRR of the proposed amplifier is 154 dB.

4. Conclusion

The proposed CMOS OTA using current buffer compensation technique in conjunction with Miller compensation technique has been employed. The Miller compensation capacitance allows the power supply ripple at the output to be large enough. Basically the proposed design is based on compensation of right half plane zero. Here the improvement in unity gain bandwidth has been done by increasing the bias current which decreases the DC gain and increases power dissipation little bit, still provides a good alternative control for an operational amplifier to operate at high frequency. The Simulation results of proposed two stages CMOS OTA are verified using S-edit and W-edit.

5. Acknowledgment

The author would like to thank for support from the Centre for Applied Research and Electronics, (CARE), IIT, New Delhi and Dept. of ECE, BIT Muzaffarnagar and Amity School of Engineering & Technology, Noidafor providing the facility to analyze and simulate the design.

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