

Modal Decomposition-based VLSI Interconnect Delay Modeling

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Abstract. In this paper we study the delay and crosstalk noise effects of multi conductor interconnect structures in nano- scale VLSI circuits employing Modal Decomposition method to decouple them. As signal rise time becomes negligible and the line resistance becomes smaller for copper interconnects, inductive and capacitive effects dominate. For the examples presented, the 50% delay using the Modal Decomposition method agrees with HSPICE results with less than 5% accuracy. The presented model matches well with the closed form delay equations.

Keywords: Capacitive and inductive coupling, Modal Decomposition, signal rise and fall times, switching patterns.

1. Introduction

The crosstalk and delay analysis in a transmission line begins with a lossless LC representation, resulting in a wave equation for the system response. To determine the effects of cross talk, delays and logic levels for the victim nets must be computed. The telegrapher's equations are applied for multi conductor lines to obtain the noise coupling using the mode decomposition technique.

Model Order Reduction (MOR) techniques [1]-[3] are employed to reduce the complexity of nanometer VLSI designs, and consequently MOR transforms a system into a circuit of much smaller size to approximate the behavior of the original description.

The paper is organized as follows: After a brief introduction in Section 1, the Modal Decomposition method and the related mathematical analysis to calculate modal inductance and capacitances are presented in section 2, while Section 3 discusses the simulation results. Conclusions are presented in Section 4.

2. Modal Decomposition method

Modal Decomposition method is used to replace the full and dense $N \times N$ inductance matrix of N interconnect lines with N linearly independent circuits. The terminal voltages and currents are broken into components corresponding to the modes of inductance matrix (Eigen vectors). The circuit behaviour of each mode is calculated separately using the modal inductances (Eigen values), and the results of all the modes are combined to obtain the complete circuit behaviour.

Using Modal Decomposition, the effect of mutual inductances is completely simulated, without actually using a mutual inductance circuit element. The per unit length inductance and capacitance matrices are decoupled to produce a Modal Decomposition. After Modal Decomposition, the circuit response is simulated using uncoupled interconnect lines. The Eigen vectors of L and C are computed, orthogonalized and normalized through application of Gram-Schmidt ortho-normalization process. Using these results L_m and C_m are calculated. The voltages and currents at each end will be transformed to modified modal voltages and currents at the ends of modal transmission lines.

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The telegrapher equations are collectively written as

$$\frac{\partial \bar{v}}{\partial z} = -\bar{r} \bar{i} - \bar{l} \frac{\partial \bar{i}}{\partial t} \quad (1)$$

And

$$\frac{\partial \bar{i}}{\partial z} = -\bar{g} \bar{v} - \bar{c} \frac{\partial \bar{v}}{\partial t} \quad (2)$$

The loss free case with $\bar{r} = \bar{g} = 0$, the voltage wave equation known as

$$\frac{\partial^2 \bar{v}}{\partial z^2} = \bar{l} \bar{c} \frac{\partial^2 \bar{v}}{\partial t^2} \quad (3)$$

The product $\bar{l} \bar{c}$ forms a square matrix that is not symmetric even though \bar{l} and \bar{c} are symmetric. However, $\bar{l} \bar{c}$ can still be diagonalized as

$$\bar{l} \bar{c} = \bar{T}_v \bar{\lambda} \bar{T}_v^{-1} \quad (4)$$

Where $\bar{\lambda}$ contains the eigen values of $\bar{l} \bar{c}$, and \bar{T}_v is constructed by orthogonal property. Substituting Eq (4) into Eq (3) and multiplying through by \bar{T}_v^{-1} yields

$$\frac{\partial^2 \bar{T}_v^{-1} \bar{v}}{\partial z^2} = \bar{\lambda} \frac{\partial^2 \bar{T}_v^{-1} \bar{v}}{\partial t^2} \quad (5)$$

Defining the modal voltages as

$$\bar{v}_m = \bar{T}_v^{-1} \bar{v} \quad (6)$$

Similarly the modal currents are

$$\bar{i}_m = \bar{T}_l^{-1} \bar{i} \quad (7)$$

Where \bar{T}_l is constructed from the eigen vectors of $\bar{c} \bar{l}$.

$$\frac{\partial^2 \bar{i}_m}{\partial z^2} = \bar{\lambda} \frac{\partial^2 \bar{i}_m}{\partial t^2} \quad (8)$$

$$\bar{c} \bar{l} = \bar{T}_l \bar{\lambda} \bar{T}_l^{-1} \quad (9)$$

The new modal inductance and capacitance matrices as

$$\bar{l}_m = \bar{T}_v^{-1} \bar{l} \bar{T}_v \quad (10)$$

And

$$\bar{c}_m = \bar{T}_l \bar{c} \bar{T}_l^{-1} \quad (11)$$

The voltages and currents at each end of multi conductor transmission line are transformed into the modal voltages and currents, which are then, propagated on decoupled transmission lines. The per unit length inductance and capacitance matrices are calculated using field solver. In this two eigen value problems must be solved. The eigen vectors of $\bar{l} \bar{c}$ are computed, orthogonalized and normalized through application of Gram-Schmidt orthonormalization process. The eigen vectors are then assembled to form \bar{T}_v . The process is

repeated for \bar{c}_l , and \bar{T}_l is formed. With \bar{T}_v and \bar{T}_l known the parameters of the decoupled lines, \bar{l}_m and \bar{c}_m , are computed.

3. Results and Discussions

The Test case examples are of five and seven conductor lines. The assumed interconnects are identical and parallel as shown in Fig1. Fig2. describes the distributed LC line. The geometrical parameters are as per Table 1. The parasitics are obtained using 2D electromagnetic field solver [6]-[8] and applied as inputs to the Modal Decomposition method, which has been implemented in MATLAB. The given diagonal matrices L_m and C_m (modal inductance and capacitance) are calculated in MATLAB. They contain only self inductance and capacitance terms, which also include the effect of mutual inductances and coupling capacitances. These diagonalised L_m and C_m matrices are presented only for seven conductors. These matrices are processed through HSPICE circuit simulator.

It is observed that, at higher rise times HSPICE delay results matched nearly with Modal Decomposition based delay, as shown in Table 2. This simple method gives acceptable results as compared to the complex method presented in [9]. For Fig.3 and Fig.4 the top waveform is input pulse waveform and bottom waveforms are HSPICE and Modal Decomposition outputs for five and seven conductor lines. Fig.3 and Fig.4 depicts that Modal Decomposition matches with HSPICE results. Fig.5 indicates the input pulse and crosstalk noises of five and seven conductor lines for third and fourth quiet victim lines. It is observed that the noise due to seven conductor lines is more due to more number of lines coupling to victim line four.

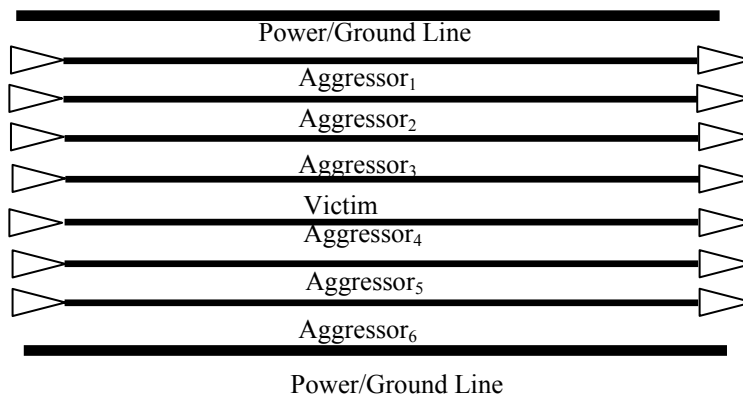


Figure 1: Seven bus line structure for the analysis of different switching patterns.

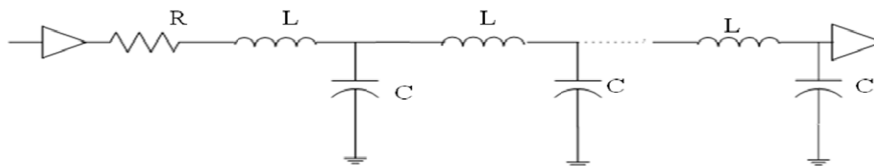


Figure 2: Distributed LC line.

Table 1: The values of circuit parameters [5]

Technology node (nm)	65
Vdd (V)	1
Minimum interconnect width (nm)	92.5
Aspect ratio = T/W	1.9
Interconnect thickness T (nm)	175.75
Dielectric thickness H (nm)	176

The Extracted inductance [pH/ μm] and capacitance [fF/ μm] matrices using HSPICE field solver

$$L=1.0\text{e-}012^* \begin{bmatrix} 0.3044 & 0.1028 & 0.0419 & 0.0199 & 0.0108 & 0.0066 & 0.0046 \\ 0.1028 & 0.2939 & 0.0989 & 0.0403 & 0.0191 & 0.0104 & 0.0066 \\ 0.0419 & 0.0989 & 0.2924 & 0.0983 & 0.0400 & 0.0191 & 0.0108 \\ 0.0199 & 0.0403 & 0.0983 & 0.2922 & 0.0983 & 0.0403 & 0.0199 \\ 0.0108 & 0.0191 & 0.0400 & 0.0983 & 0.2924 & 0.0989 & 0.0419 \\ 0.0066 & 0.0104 & 0.0191 & 0.0403 & 0.0989 & 0.2939 & 0.1028 \\ 0.0046 & 0.0066 & 0.0108 & 0.0199 & 0.0419 & 0.1028 & 0.3044 \end{bmatrix}$$

$$C=1.0\text{e-}016^* \begin{bmatrix} 0.7299 & -0.1587 & -0.0096 & -0.0041 & -0.0023 & -0.0015 & -0.0014 \\ -0.1587 & 0.7826 & -0.1556 & -0.0083 & -0.0034 & -0.0019 & -0.0015 \\ -0.0096 & -0.1556 & 0.7828 & -0.1555 & -0.0083 & -0.0034 & -0.0023 \\ -0.0041 & -0.0083 & -0.1555 & 0.7829 & -0.1555 & -0.0083 & -0.0041 \\ -0.0023 & -0.0034 & -0.0083 & -0.1555 & 0.7828 & -0.1556 & -0.0096 \\ -0.0015 & -0.0019 & -0.0034 & -0.0083 & -0.1556 & 0.7826 & -0.1587 \\ -0.0014 & -0.0015 & -0.0023 & -0.0041 & -0.0096 & -0.1587 & 0.7299 \end{bmatrix}$$

The new modal inductance [pH/ μm] and capacitance [fF/ μm] matrices are calculated as

$$L_m = 1.0\text{e-}012^* \begin{bmatrix} 0.4232 & 0.0000 & -0.0000 & -0.0000 & -0.0000 & -0.0000 & -0.0000 \\ -0.0000 & 0.5702 & -0.0000 & -0.0000 & 0.0000 & -0.0000 & -0.0000 \\ 0.0000 & 0.0000 & 0.3149 & -0.0000 & -0.0000 & 0.0000 & -0.0000 \\ 0.0000 & 0.0000 & 0.0000 & 0.2423 & 0.0000 & -0.0000 & 0.0000 \\ -0.0000 & -0.0000 & 0.0000 & -0.0000 & 0.1970 & 0.0000 & 0.0000 \\ 0.0000 & -0.0000 & -0.0000 & -0.0000 & -0.0000 & 0.1553 & -0.0000 \\ -0.0000 & -0.0000 & 0.0000 & -0.0000 & -0.0000 & 0.0000 & 0.1698 \end{bmatrix}$$

$$C_m = 1.0\text{e-}015^* \begin{bmatrix} 0.0549 & -0.0000 & 0.0000 & 0.0000 & 0.0000 & 0.0000 & 0.0000 \\ 0.0000 & 0.0471 & 0.0000 & 0.0000 & 0.0000 & 0 & -0.0000 \\ -0.0000 & -0.0000 & 0.0650 & 0.0000 & 0.0000 & -0.0000 & 0.0000 \\ -0.0000 & -0.0000 & -0.0000 & 0.0768 & -0.0000 & 0.0000 & -0.0000 \\ 0.0000 & 0.0000 & -0.0000 & 0.0000 & 0.0887 & -0.0000 & -0.0000 \\ -0.0000 & 0.0000 & 0.0000 & 0.0000 & 0.0000 & 0.1057 & 0.0000 \\ 0.0000 & 0.0000 & -0.0000 & 0.0000 & 0.0000 & -0.0000 & 0.0989 \end{bmatrix}$$

Table 2: Rise time vs delay for aggressor same and opposite direction switching patterns

Switching of Aggressor	Rise time (in ps)	Delay (in ps)		Error (%)
		SPICE	Modal Decomposition	
Same	10	13.5	14.1	4.4
	50	10.07	10.16	0.89
Opposite	10	5.1	5.24	2.7
	50	9.16	9.26	1.09

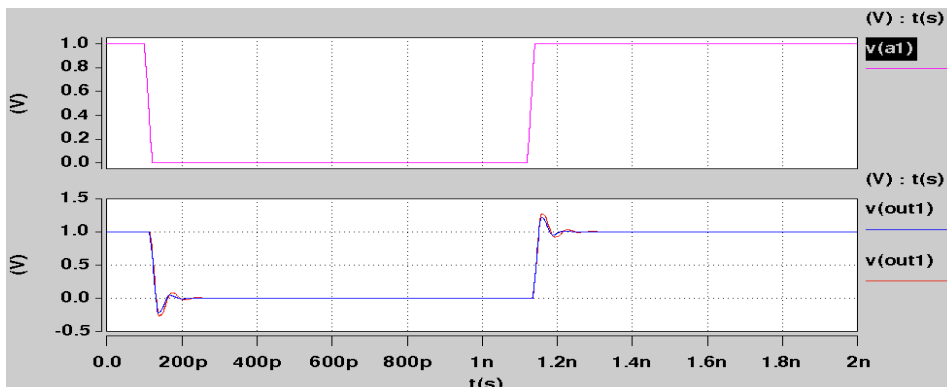


Figure 3: Input pulse, HSPICE (maroon) and Modal Decomposition (blue) results for five conductor lines.

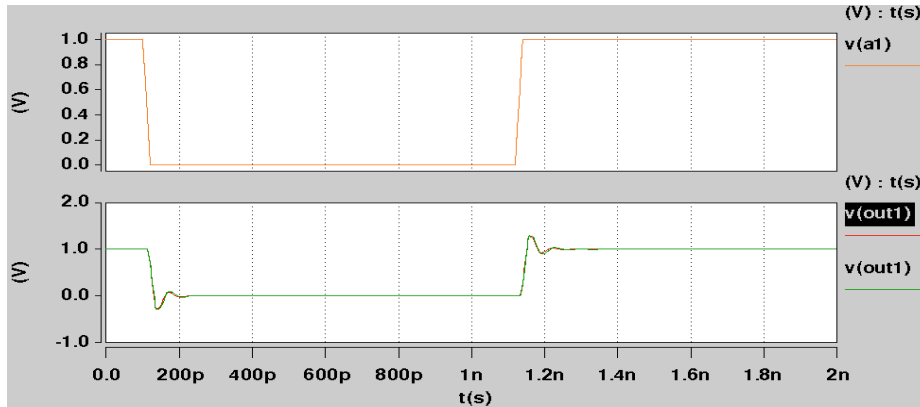


Figure 4: Input pulse, HSPICE (maroon) and Modal Decomposition (green) results for seven conductor lines.

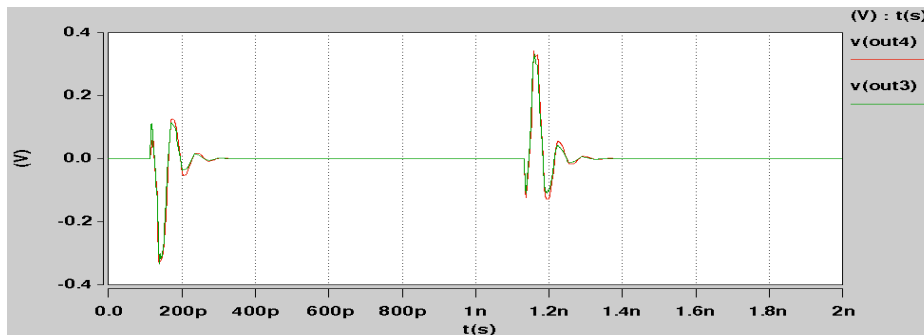


Figure 5: Crosstalk for seven (large peak) and five (small peak) conductor lines for same input pulse of 1v.

4. Conclusion

In this paper we have presented an efficient, simple and accurate delay model for on chip VLSI interconnects using Modal Decomposition. Modal inductance and capacitance equations have been derived and the on chip interconnect is modeled as distributed LC line. Results from the presented method are in very good agreement with the ones from HSPICE simulations with less than 5% error. This method can be used for VLSI non- uniform interconnect analysis and design. The accuracy of the present model has been verified by comparing its results with those obtained using other methods.

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