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SV PWM Pattern Generator using Field Programmable Gate Array Implementation

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Abstract. This paper presents an application of FPGA producing Pulse Width Modulation with a vector modulation technique for an inverter. The successful application of Space Vector Pulse Width Modulation (SVPWM) for a three phase VSI and it is the standard PWM techniques to utilize the DC-AC power conversion. SVPWM techniques enjoy an assortment of advantages such as high output quality, less THD, low distortion and low rating filter component. In addition, SVPWM technique offers flexible control of output voltage as well as frequency, which is indeed requirement in ac drives with line current sinusoidal in nature and thus improving the overall power factor of the system. Hence, to obtain good voltage transfer and reduced distortion Space Vector PWM is required. Space vector PWM can produce about 15 percent higher output voltage than standard Sinusoidal PWM. Field programmable gate arrays (FPGAs), with their concurrent processing capability, are suitable for the implementation of multilevel modulation algorithms. Among them, space vector pulse width modulation algorithms offer great flexibility to optimise switching waveforms. Using a single FPGA chip for the practical implementation, rather than a system consisting of microprocessor and external memory, has many advantages including less use of power and space, short design time, greater speed and reliability. FPGA is chosen due to its fast prototyping, simple hardware and software design.

Keywords: Field programmable gate array (FPGA), three-phase voltage source inverter, space vector pulse width modulation (SVPWM), Printed circuit board (PCB).

1. Introduction

PWM inverters are becoming more and more popular in today's motor drives. As a result, PWM inverter powered motor drives offer better efficiency and higher performances compared to fixed frequency motor drives. Sinusoidal Pulse Width Modulation (SPWM), is used to control the inverter output voltage and maintains a good performance of the drive in the entire range of operation between zero and 78 percentage of the value that would be reached by square operation. In the other hand, Space Vector Modulation Techniques have been increased by using in last decade, because they allow reducing commutation losses and the harmonic content of output voltage, and to obtain higher Amplitude modulation indexes if compared with convectional SPWM techniques. The Pulse Width Modulation (PWM) Technique called "Vector Modulation", which is based on space vector theory, is the most important development in the last few years.

Space Vector Modulation (SVM) was originally developed as a vector approach to pulse width modulation (PWM) for three phase inverter. Field programmable gate arrays (FPGA's) are standard integrated circuits that can be programmed by a user to perform a variety of complex logic functions. The high level of integration available with these devices (currently up to 500,000 gates) means that they can be used to implement complex electronic systems.

This paper presents a space vector pulse width modulation for an inverter circuit which drives the three phase induction motor. The SVPWM pulses are thus generated by developing VHDL coding burnt in the

FPGA kit and the triggering pulses are viewed by using the Xilinx software. Therefore this paper is a real time implementation.

Thus the work is divided into 3 main sections.(I)the FPGA kit along with the coding(II)the driver circuit which acts as the interfacing circuit board between the FPGA and the power electronics circuit board (III)which consists of the hardware circuit of an three phase voltage source PWM inverter and the three phase motor.

2. Principle of Pulse Width Modulation (PWM)

The Fig.1 shows circuit model of a single-phase inverter with a center-taped grounded DC bus

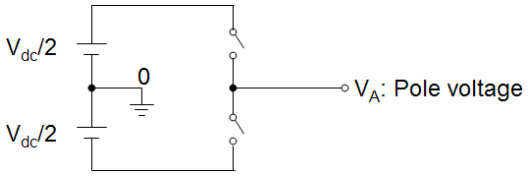


Fig 1. Circuit model of a single-phase inverter

It illustrates the principle of pulse width modulation

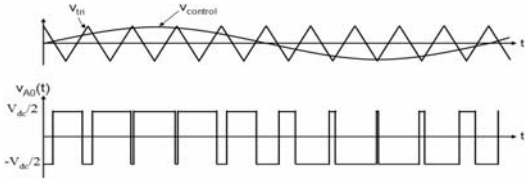


Fig 2. Pulse width modulation.

As depicted in Fig., the inverter output voltage is determined in the following:

- When Vcontrol > Vtri, VA0 = Vdc/2
- When Vcontrol < Vtri, VA0 = −Vdc/2

3. Principle of Space Vector PWM

The circuit model of a typical three-phase voltage source PWM inverter is shown in Figure below. S1 to S6 are the six power switches that shape the output, which are controlled by the switching variables a, a', b, b' and c, c'. When an upper transistor is switched on, i.e., when a, b or c is 1, the corresponding lower transistor is switched off, i.e., the corresponding a′, b′ or c′ is 0. Therefore, the on and off states of the upper transistors S1, S3 and S5 can be used to determine the output voltage.

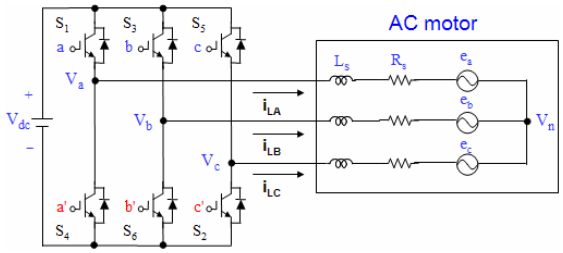


Fig 3. Three-phase voltage source PWM Inverter

There are eight possible combinations of on and off patterns for the three upper power switches. According to equations and, the eight switching vectors, output line to neutral voltage (phase voltage), and output line-to-line voltages in terms of DC-link Vdc, are given in the Table and next Figure shows the eight inverter voltage vectors (V0 to V7).

Table 1: Switching vectors, phase voltages and output line to line voltages

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

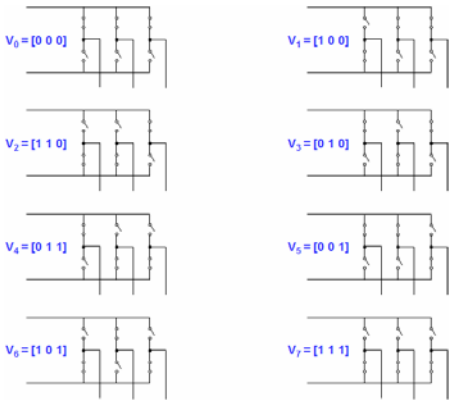


Fig. 4: The eight inverter voltage vectors (V0 to V7)

Space Vector PWM (SVPWM) refers to a special switching sequence of the upper three power transistors of a three-phase power inverter

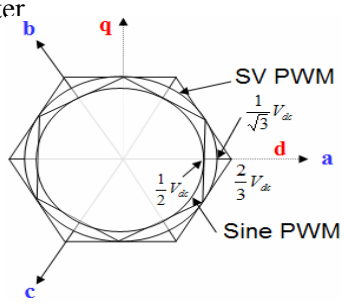


Fig. 5: Locus comparison of maximum linear control voltage in Sine PWM and SVPWM.

To implement the space vector PWM, the voltage equations in the abc reference frame can be transformed into the stationary dq reference frame that consists of the horizontal (d) and vertical (q) axes as depicted in Figure:

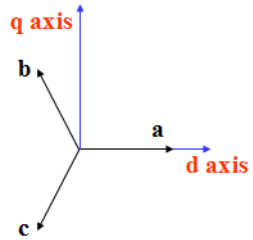


Fig. 6: The relationship of abc reference frame and stationary dq reference frame.

As described in Figure, this transformation is equivalent to an orthogonal projection of [a, b, c]t onto the two-dimensional perpendicular to the vector [1, 1, 1]t (the equivalent d-q plane) in a three-dimensional coordinate system. The eight vectors are called the basic space vectors and are denoted by V0, V1, V2, V3, V4, V5, V6, and V7. The objective of space vector PWM technique is to approximate the reference voltage vector Vref using the eight switching patterns.

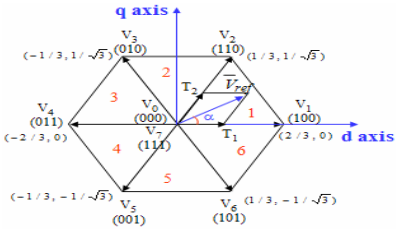


Fig. 7: Basic switching vectors and sectors

Therefore, space vector PWM can be implemented by the following steps:

- Step 1. Determine Vd, Vq, Vref, and angle (α)
- Step 2. Determine time duration T1, T2, T0.
- Step 3. Determine the switching time of each transistor (S1 to S6).

4. Field Programmable Gate Array

A Field-Programmable Gate Array or FPGA is a silicon chip containing an array of configurable logic blocks (CLBs). The design used Xilinx development tools, namely Workview, and is realized in a single FPGA chip with no external memory. The benefits of this design are as follows:

- The whole system is implemented in only a single chip consequently the circuit is very compact.
- Systems on a FPGA chip are more reliable because they do not need any control software.
- Faster design and verification time, design change without penalty.

In this paper programming FPGA using Hardware Description Languages and coding are used to generate the Space Vector Modulation for the inverter circuit. The Hardware Description Language is familiar to the vast number of software programmers and since VHDL is very much common to most of the programmers it becomes easier for individuals to work in this software.A very attractive high-level design/simulation tool is provided by FPGA and is called XILINX.

Simulation Steps:

1). Initialize system parameters using FPGA
2). Perform VHDL coding to

- Determine sector
- Determine time duration T1, T2, T0
- Determine the switching time (Ta, Tb, and Tc) of each transistor (S1 to S6)
- Generate the inverter output voltages (ViAB, ViBC, ViCA,) for control input (u)
- Burn the program in the FPGA kit

3) View the SVPWM waveforms through xilings

5. Simulation Result

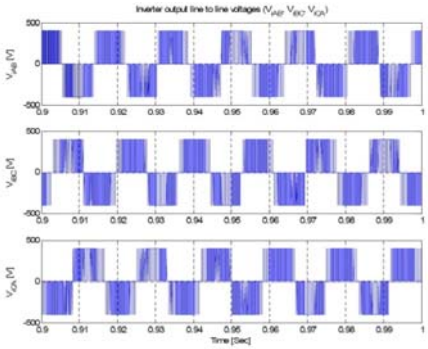


Fig. 7: Simulation results of inverter output line to line voltages

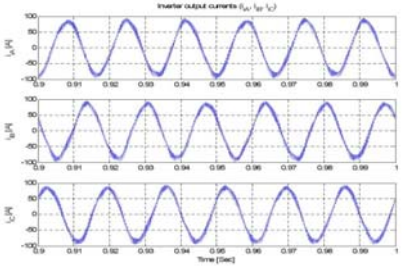
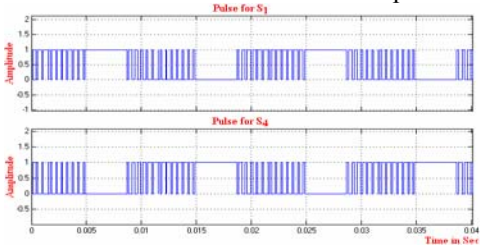


Fig. 8: Simulation results of inverter output currents



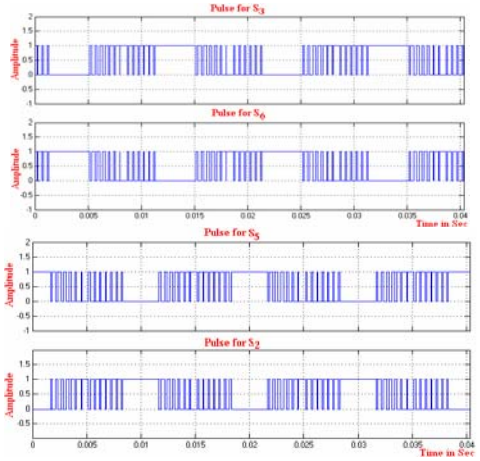


Fig. 9: Triggering SVPWM pulses for the VSI circuit from FPGA

6. Conclusion

In this paper, a theoretical study concerning the SVPWM control strategy on the voltage inverter based on FPGA is presented. This aims on the one hand to prove the effectiveness of the SVPWM in the contribution in the switching power losses reduction. SVPWM is among the best solution to achieve good voltage transfer and reduced harmonic distortion in the output of an inverter.

Since Field programmable gate array (FPGA) have better advantages compared to microprocessor and DSP control, this modulation technique is implemented in an FPGA. The FPGA coding makes it easier in designing the vector modulation pattern generator using field programmable Array.

7. Acknowledgements

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8. References

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