

Analog Front End Design of Contactless Smart Card

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Abstract. This paper describes a new set of analog front end circuit design proposal for contactless smart card which complies with ISO/IEC 14443-2 Type A. It has been implemented in SMIC 0.18um eflash process successfully. The packaged chip can operate well at 13.56MHz with data rate of 106Kbps. And its performance has been considerably improved on the basis of former version. The simulation result and test result will be listed in the following thesis.

Keywords: RFID, Contactless, Power recovery, Rectifier, Limiter, Demodulator, Modulator, POR.

1. Introduction

Radio-frequency identification (RFID) is a technology that uses radio waves to transfer data from an electronic tag, called RFID tag, attached to an object, through a reader for the purpose of identifying and tracking the object [1]. RFID emerged in 1990s and has developed rapidly in recent years. Contactless smart card is a core technology of RFID, which is more favored for its long operating distance, high efficiency and ideal convenience comparing with contact card technology. Contactless smart card market enters a new era, with a booming number of applications in various domains such as commerce, administration, public transportation and so on. Its systems are characterized by three elements: the reader, the card and the transmission channel. This paper describes the analog front end circuit design for PICC which complies with ISO/IEC 14443-2 Type A. The design satisfies the demands of test protocol and has been fabricated in SMIC 0.18um eflash process successfully.

2. Design Standard

ISO/IEC 14443 specifies the characteristics of the fields to be provided for power and bidirectional communication between proximity coupling devices (PCDs) and proximity integrated circuit cards (PICCs) [2]. PCD modulates the amplitude of the alternating magnetic field strength with modulation pulses, in order to transmit data from PCD to PICC. According to the ASK modulation index, 14443-2 defines two communication signal interfaces, Type A and Type B. The signal of Type B from PCD to PICC is modulated in ASK with modulation index 10%, while Type A is 100%. Either option has its advantages and disadvantages, although Type B has higher responding speed and higher security because of the continuous power supply, Type A has much larger market penetration rate. This paper adopts the solution given by Type A.

3. Circuit Design

Contactless smart card contains two main sections, one is analog front end, and the other is digital logic and memory. This paper focuses on the former, which consists of five parts: power recovery module (composed of full-wave rectifier and limiter), demodulator, clock gen, modulator, and power detect module. The basic structure of analog front end is showed in Fig.1.

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If we regard limiter in Fig.2.(b) as a unit, one more unit is added to the new structure called two-stage limiter. As is showed in Fig.3.(a), digital logic adjusts the 8bits to control I , that is also the current of M7, used as mirror reference. The right path including M8 can obtain $m \cdot I$ mirror current by setting appropriate sizes of M7 and M8. As digital logic knows what it will do next and how much energy it will need, it can adjust suitable 8bits in advance to acquire sufficient energy. Furthermore, the ripple of VDD from PWR1 is suppressed greatly because of the cascade structure's shielding property. In addition, the chip needs a large number of caps to live through the energy pause during the communication course between PCD and PICC. Fig.3.(b) is the simulation results of VDD under different operating loads with two-stage limiter.

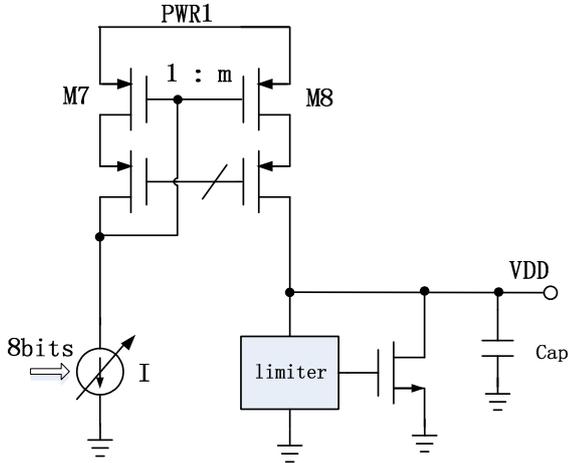
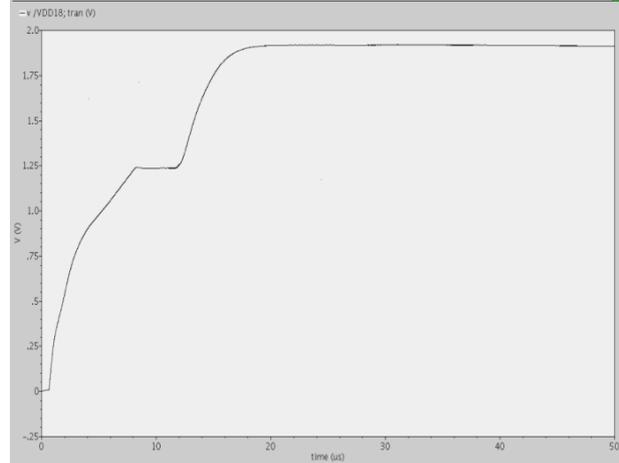


Fig.3. (a) Circuit of two-stage limiter;



(b) Simulation result of VDD under different operating loads

3.2. Demodulator

The demodulator recovers digital signals from the 100%ASK signal transmitted by PCD. An envelope detector and a voltage reference are needed in conventional way, in this paper we propose a new demodulator suitable for any magnetic density stated by ISO/IEC 14443-2. Adopting edge detection, this new method first lets the same signal pass two paths with different time constants, and then compares the outputs of the two paths. As is indicated in Fig.4.(a), we use a sample of the output of first stage limiter (V_{IN}) as the input of this new demodulator. The DC of V_{IN} remains at a certain value when PCD emits surplus energy, and falls down sharply as soon as the energy pause comes. Then the hysteresis comparator compares the separated signals after different RCs [3]. Hence data is recovered from the 100%ASK signal, and then given to digital for next processing.

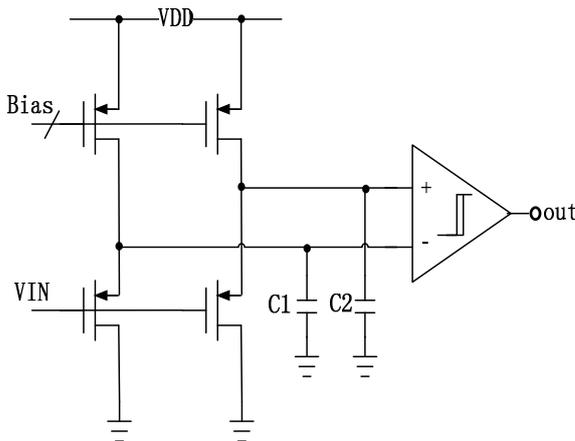
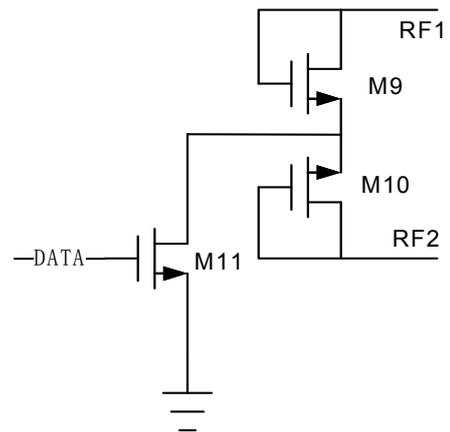


Fig.4. (a) Circuit of demodulator;



(b) Circuit of modulator

3.3. Clock Gen

As there is no local oscillator, analog front end is required to provide clock signal for digital logic section. Clock gen can recover clock signal of 13.56MHz from electromagnetic waves by several inverters using RF1 as the input signal. After follow-up processing of digital divider, the output signals can be used as system clock and subcarrier.

3.4. Modulator

The modulating approach is determined by the methods of RF signal coupling, here we adopt load modulation to transmit data from PICC to PCD. Traditional way is to change the transmitting parallel capacitor in order to affect its coupled voltage. This way inevitably changes the coupled resonant LC network, as a result, power supply efficiency is badly affected. We propose a new method by modulating the impedance paralleled across the antenna as the above Fig.4.(b). Digital logic generates subcarrier of 847KHz by dividing carrier of 13.56MHz, then uses digital signal to modulate the subcarrier with BPSK [4]. In analog front end, the modulated subcarrier (DATA in Fig.4) controls the amount of discharging current through M11 to change the amplitude of RF.

Fig.5.(a) is a graph traced by the oscillograph when we test the smart card in MicroPross MP300 TCL2 Tester with Universal Test Bench. It shows the RF waves when PICC transmitting DATA to PCD.

4. Performance and Conclusion

In the course of this design, each module and the whole chain are simulated in the SMIC 0.18um CMOS technology library. Within the energy scope of PCD can provide, the new structure power recovery module can obtain as much energy as digital logic wants by adjusting the 8bits control word. The value of VDD remains consistent under different loads, and the ripple of VDD is especially small when digital logic switches its operative mode quickly. Power detector will send a high level signal to digital section when VDD reaches 1.7V, and give a falling edge (Power-down-reset) when VDD decreases to 1.55V. The demodulator can recovers data from the electromagnetic field correctly even under 1A/m.

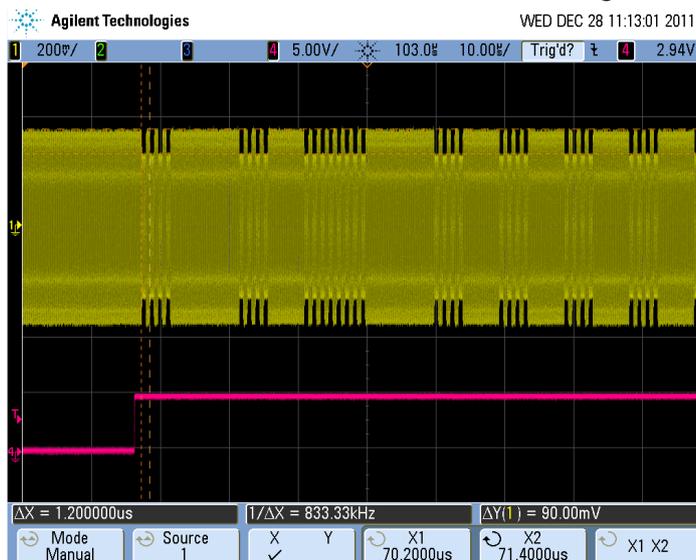
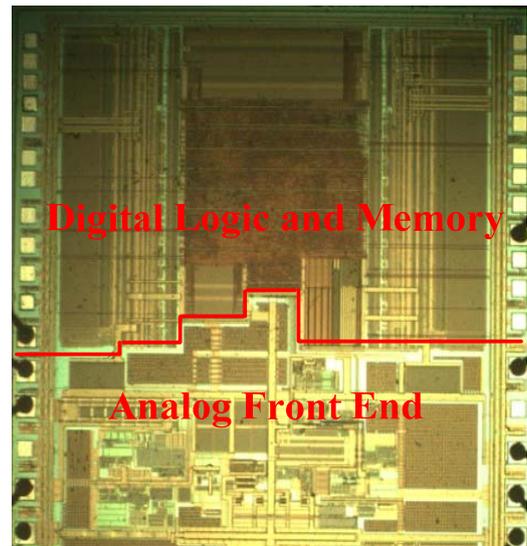


Fig.5.(a) Test result of modulator



(b) Die photo of the chip

The design above has been successfully implemented in SMIC 0.18um eflash process. Fig.5.(b) shows the die photo of smart card chip. Large quantities of testing proves that contactless smart card with this design operates well at 13.56MHz with the data rate of 106Kbps in all the field strength according to ISO/IEC 14443-2.

5. References

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