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Proposed Multiplier with Low Power and Efficient Performance

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Abstract. Analog multipliers found its wide spread applications in the era of signal processing, neural networks as well as frequency doublers, RMS circuits and phase detectors (phase lock loop). High input signal range, linearity and high operating frequency are the prime issues for the multipliers in conventional applications like modem modulation circuits. Power consumption is the criteria in case of massive parallel processing based networks. In this paper, a CMOS analog multiplier, with less number of transistors which can operate at high frequencies with low power and high linearity is proposed. The multiplier works on the basis of parallel connected MOS operation circuit. The circuit is designed and simulated using TSPICE simulator by level 49 in 180nm standard CMOS technology at power supply of 1V.

Keywords: CMOS, Multipliers, Power consumption, DC gain.

1. Introduction

A multiplier is an important component for many analog applications. An analog multiplier is a device which takes two analog signals and produces an output which is their product. Such circuits can be used to implement related functions such as squares (apply same signal to both inputs), and square roots. Due to the popularity of advanced CMOS technology, MOS transistors are a natural choice for the devices, while differential circuit structure is widely used for nonlinearity cancellation. In this paper, we present a new multiplier with CMOS structure with emphasis on low power consumption. We analyze various performance metrics of the multiplier and provide some design considerations. It is demonstrated in particular that this multiplier is much better than other structures in terms of power consumption, and is hence especially suitable for implementation of large-scale circuits. This multiplier is termed a four-quadrant multiplier because both inputs can be either positive or negative around a common-mode voltage, V_{CM}. The outputs of the multiplier is related to the inputs by [1]

$$V_o = K_m . v_x v_y \tag{1}$$

Where K_m is the multiplier gain with units of V^{-1}.

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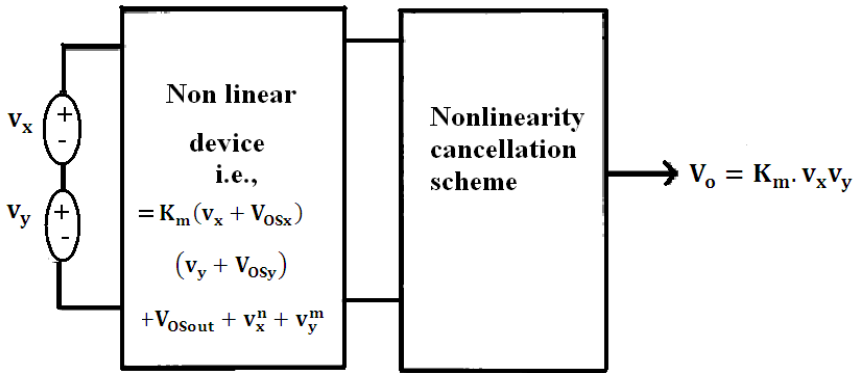

Fig.1: Basic idea of Multiplier

In reality, imperfections exist in the multiplier gain, resulting in offsets and nonlinearities. The output of the multiplier can be written as

$$V_o = K_m(v_x + V_{OSx})(v_y + V_{OSy}) + V_{OSout} + v_x^n + v_y^m \quad (2)$$

2. Four-Quadrant Multipliers using Series Connected Transistors

A voltage mode four quadrant analog multiplier based on a basic NMOS differential amplifier[1] that can produce the output signal in voltage form can be constructed using four one-quadrant multipliers or by using two two-quadrant multipliers.

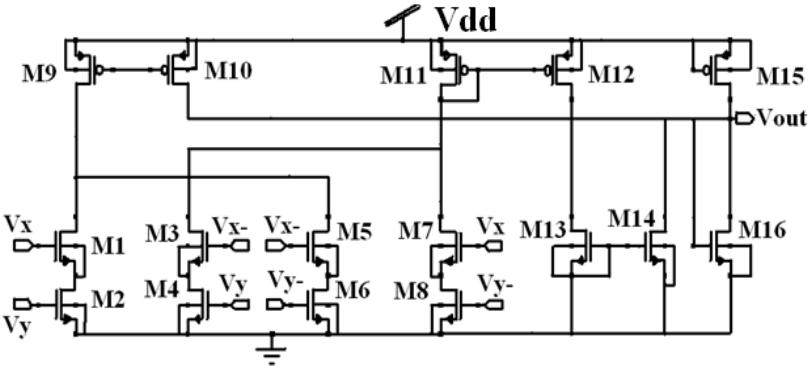

Fig.3: Schematic of Four Quadrant Voltage Mode Multiplier

Since it has to operate in all the quadrants, output of $V_X \times V_Y$ and $-V_X \times -V_Y$ are cross connected to get the total current I_{total1} and similarly the output of $-V_X \times V_Y$ and $V_X \times -V_Y$ are cross connected to get the total current I_{total2}.

3. Proposed Multiplier

Here we present a low voltage, low power, high linearity and high speed multiplier circuit which operates in the voltage mode using parallel connected MOS devices at the input side and diode connected MOS devices as a load at the output side. Fig.4 shows how transistors can be used to implement multipliers. In order to reduce the number of devices parallel structure is useful compared to cascaded structure. The basic block diagram of four quadrant voltage mode multiplier is shown in Fig.5. The purpose of

implementing this structure is to reduce the number of devices with minimum size. In this design, instead of using NMOS at the load side PMOS are used because of its negative threshold voltage.

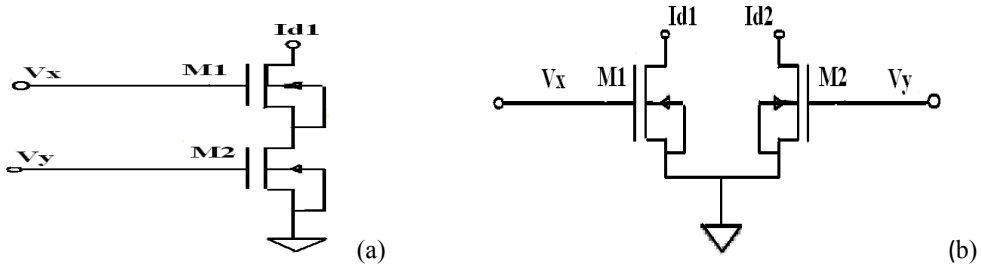

Fig.4: Shows the basic circuit configurations (a) Cascade structure (b) Parallel structure

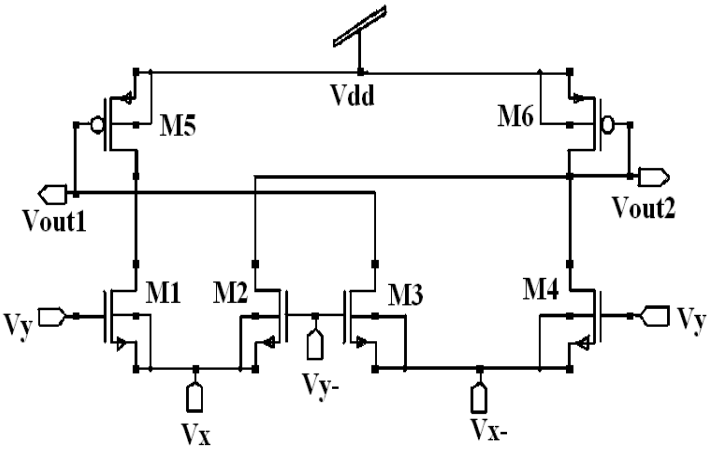

Fig.5: Modified Four Quadrant Multiplier Structure

Since transistors are operating in the triode region, let us consider the equation for small signal model [4].

$$i_d = K'V_{ds}V_{gs} \tag{7}$$

$$i_{d_1} = K'V_{ds_1}(V_x - V_y) \tag{8}$$

$$i_{d_2} = K'V_{ds_2}(-V_y - V_x) \tag{9}$$

$$i_{d_3} = K'V_{ds_3}(-V_y + V_x) \tag{10}$$

$$i_{d_4} = K'V_{ds_4}(V_y + V_x) \tag{11}$$

$$i_{d_1} + i_{d_3} = K'\left[\left(-2V_xV_y\right) + \left(2V_x^2\right)\right] \tag{12}$$

$$i_{d_2} + i_{d_4} = K'\left[\left(2V_xV_y\right) + \left(2V_x^2\right)\right] \tag{13}$$

$$\left(i_{d_2} + i_{d_4}\right) - \left(i_{d_1} + i_{d_3}\right) = 4K'V_xV_y \tag{14}$$

Above equation shows that the output of multiplier is depends on the trans-conductance parameter, which in turn depends on the threshold voltage and W/L ratio of the device.

4. Simulation Results

Output of the multiplier is differential output and is as shown in Fig.7 i.e. V_{out}= ($V_{o1} - V_{02}$) and is obtained by setting $V_{x1} = V_{x2}$ =1GHz and $V_{y1} = V_{y2}$ =10GHz. Input signals are shown in Fig.6. Common mode noise gets eliminated completely because of differential output. Frequency response of this modified multiplier is shown in Fig.8. It achieves the dc gain of 11.62dB. Power results are also considered in the simulation results.

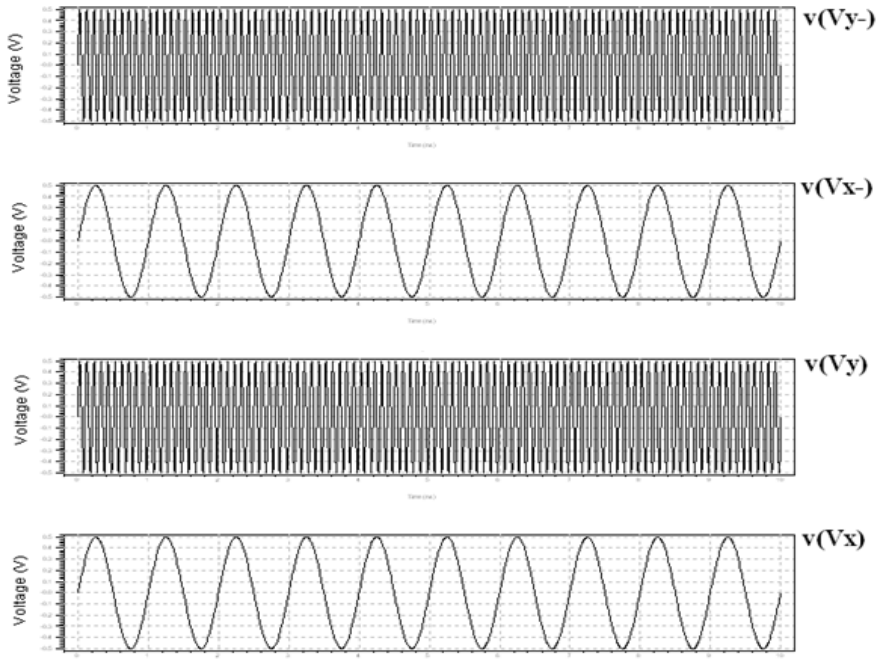

Fig.6 Inputs to the Modified Multiplier

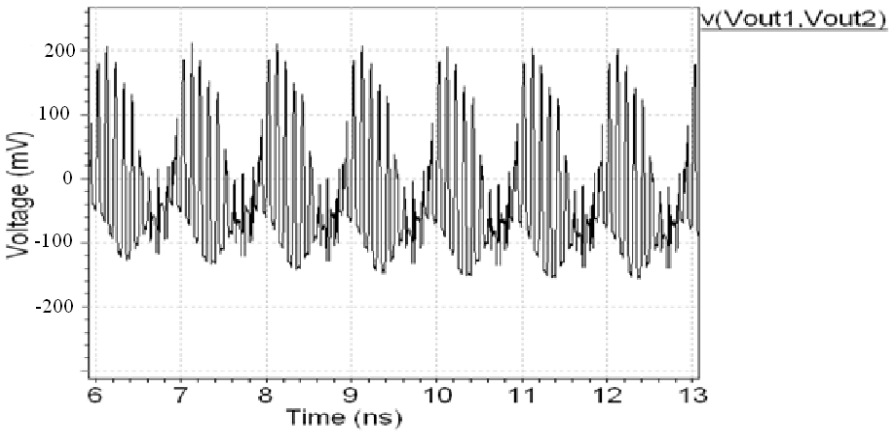

Fig.7 Output of modified Multiplier

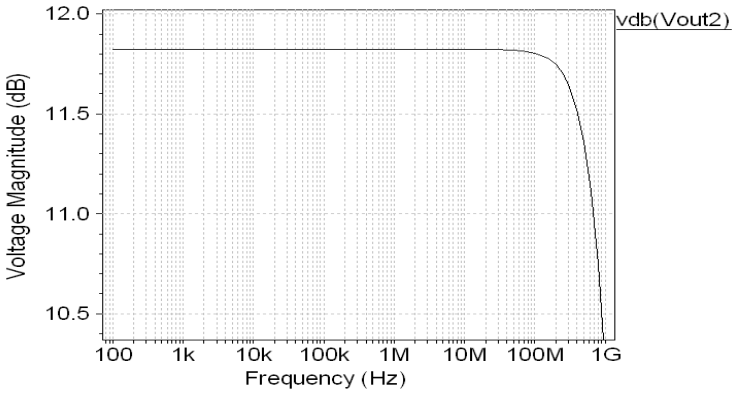

Fig.8 Frequency Response of Modified Multiplier

5. Conclusion

All the multiplier circuits are implemented in 180nm technology with minimum transistor sizes (W/L=180nm/180nm). It can be operated even at low Supply voltage V_{DD}=1V. The circuit is designed using 180nm-TSMC MOSIS Level- 49 model and then simulated using TSPICE (SPICE Simulator), W-Edit for waveform capture.

The linearity, supply voltage, power dissipation and area are the main metrics of performance. We try to design some specific structures or topologies for the analog multiplier that have low power dissipation while at the same time improving dc gain and minimizing area. Modified multiplier is designed by six transistors only which reduces the area and power consumption by maintaining the same results as conventional multiplier. DC gain of this multiplier is also improved by the value 19.62dB.The power consumed by the modified multiplier is 69µW.Therefore the proposed structure with less number of transistors occupies less area and hence consumes less power.

6. References

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