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A Modular Approach to VGA Monıtor Controller for BZK.SAU.FPGA10.1 Microcomputer Archıtecture Design

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Abstract. In this paper, we have adopted the modular approach to VGA monitor controller for BZK.SAU.FPGA10.1 [1] microcomputer architecture design developed for supporting undergraduate courses in computer science and related discipline. This modular VGA monitor controller is developed to write programs in the assembler interface of our microcomputer architecture and entirely realized using schematic structure on Altera's Cyclone II development board. It allows being able to type our assembly programs on a screen instead of writing the machine code manually. In this way, it is easer to handle errors transparently on the screen than examining the machine code one by one. Although every character in this controller is represented 8x16 pixels, the size of character can easily change through this modular structure. Also the user can include their own characters to user reserved section in the memory of our microcomputer architecture. Because of this feature, it is possible to display characters not only the languages using Roman alphabet such as Turkish, English etc. but also the languages using special alphabet such as Chinese using VGA monitor controller. So the use of BZK.SAU.FPGA10.1 microcomputer architecture design with this feature will be increased as an educational tool. Also teachers can teach more productive course by including this modular VGA controller to our microcomputer architecture design.

Keywords: VGA Monitor Controller, FPGA, Microcomputer Architecture Design, Educational Tool, Microprocessor, Modular Approach

1. Introduction

VGA(Video Graphics Array) is the most popular interface in many enbedded systems widely. It provides for users to show information, or to interact with a aystem. VGA monitor controller is a logic circuit to control VGA intrface signals. It uses color and synchronization signals of VGA interface to display an information on screen. An information is displayed on the screen by turning on and off individual pixels[5]. Whole information re-drawn at refresh rate for ensuring visual quality. The frequency of every pixel changes according to display resolution and refresh rate. As a result of this, higher fresh rates and better resolutions will require higher pixel frequency. There are a detailed information about VGA in [6]

This circuit can be realized using FPGA, which is the popular technology widely, with a low cost and high flexibility. There are several FPGA-based designs of VGA monitor controller[2-4]. They provide plenty of features. All of these designs are realized using software programming language, such as VHDL, Verilog etc. The design in [5] is only implemented using schematic design on Altera UP2 development board. It has very useful information about the working of VGA monitor. It writes to screen certain characters since it does not have a keyboard support.

This paper introduces a modular approach to VGA monitor controller for BZK.SAU.FPGA10.1 microcomputer architecture. The rest of this paper is organized as followed. Section 2 presents the general information about our architecture. Section 3 introduces the architecture of VGA monitor controller module. Finally, Section 4 concludes some achievement of this work.

2. BZK.SAU.FPGA10.1 Microcomputer Architecture

The BZK.SAU.FPGA10.1 is the new version of BZK.SAU.FPGA10.0 [8]. We have adopted the modular approach to the second FPGA version of the BZK.SAU [7] named BZK.SAU.FPGA10.1 [1]. [7] and [8] have the same architecture. The only difference between them the development environments. While the development environment of [8] is FPGA, other is an emulator program.

Modular design is an important factor for the educational training of micro computer architecture. We took the approach of modularization in order to avoid having students be overwhelmed by the complexity of a complete computer system design. Since it has modular nature, students do not have to build a microcomputer architecture from scratch. In this approach, it is quite simple to include their designs like adding unit, subtraction unit etc. to our system. So they can see the operation of their own designs on our system. In other words, our modular approach is ***plug&see***. Therefore, teachers can teach more productive course by applying this approach to their teaching methods since our approach aims to learn piece by piece rather than complete system. All units in BZK.SAU.FPGA10.1 microcomputer architecture are our own specific designs and we built these units using only schematic design at logic level. A detailed block diagram that shows the components of the BZK.SAU.FPGA10.1 design is shown in Fig. 1.

The common features of both versions are listed as the following:

a) Support six addressing modes: immediate, direct, indirect, index, relative and inherent mode.

b) It has eight general and special registers: Address Register(AR), Data Register(DR), Accumulator(AC), Program Counter(PC), Stack Pointer(SP), Index Register(IX) and Temporary Register(TR) are 16-bit; Instruction Register(IR), Output Register(OUTR) and Input Register(INPR) are 8-bit.

c) 16-bit data bus and address bus.

d) The instructions which have relative and index addressing modes need an effective address. So, it has a unit that calculates this address.

e) The instruction set consists of 51 instructions: 21 instructions for memory and accumulator, 8 instructions on index and stack registers, 22 instructions to change the flow direct of program execution.

f) 64 KB main memory for running programs and 8 MB flash memory for storing files.

g) The output pixel size of display screen on VGA monitor is 320x384 pixels and screen area has 40 columns x 24 rows since every character is 8x16 pixels.

Instructions that use direct, immediate, indirect addressing modes occupy 3 bytes to execute in the memory. Instructions that use index and relative addressing modes occupy 2 bytes to execute while inherent addressing mode instructions occupy 1 byte to execute. In order to provide readers with the detailed features of instructions and instruction structures, more data are given [1,7,8].

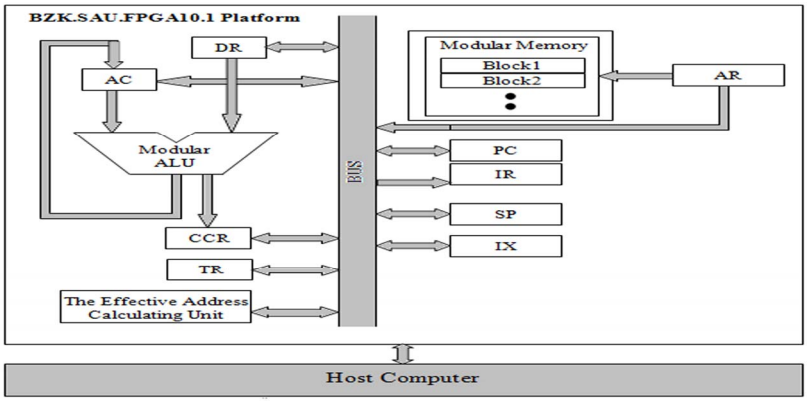

Fig.1 The Block diagram of BZK.SAU.FPGA10.1[1]

3. The Architecture of Vga Monitor Controller Module

In this section, the architecture of VGA monitor controller module developed for BZK.SAU.FPGA10.1 microcomputer architecture is illustrated. In order to run programs on our architecture was used software-

based interactive system[9]. This interactive system was written using C# programming language in the Microsoft Visual Studio .NET platform. The source program was written in the assembler section of this interactive system according to our assembler rules and sent to BZK.SAU.FPGA10.1 microcomputer architecture through RS-232 interface. This approach is not suitable in terms of creating original system. So we have included VGA monitor controller to write our source programs on the own hardware of our microcomputer achitecture. Also this controller can be used to display the information/image separately. The VGA monitor controller is controlled by five control signals: red, green, blue, horizontal synchorization and vertical synchronization. These control signals are only built two 10-bit binary-up counter for real column and row numbers and four S-R flip-flop. It is given a detailed information about how to build the control circuit of them[5].

We have adopted to our VGA monitor controller circuit these control signals. The size of our screen area is 320x384 pixels because of the deficieny of memory of our architeecture. The number of column and row in this area is 40 and 24 respectively. The starting and finish points of this display screen are shown Fig.2.

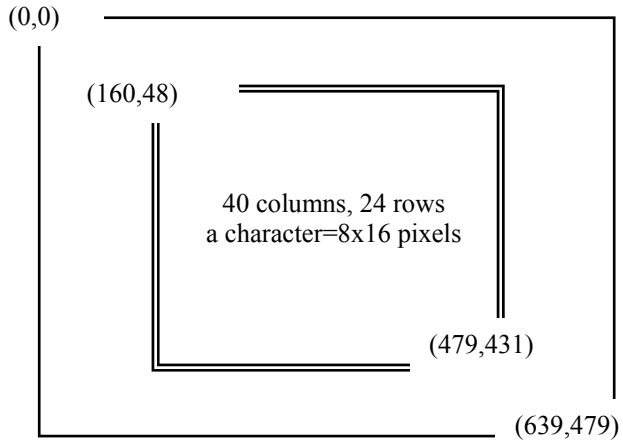

Fig.2 The desired screen area

It has six sections: column pointer, row pointer, row pixel pointer, column pixel pointer, address calculating unit and In-out screen control unit. These units are developed for our architecture design. Whole units are realized using only schematic design at logic level using Altera's Quartus II software program.

Column pointer: Points column number of the cursor. This unit is actually modulus 40 counter.

Row pointer: Points row number of the cursor. It is modulus 24 counter.

Column pixel pointer: Points column pixel number of every character. It is modulus 8 counter.

Row pixel pointer: Points row pixel number of every character. It is modulus 16 counter.

Address calculating unit: Calculates the address according to above values of pointers. This address is used to store memory the bitmap of pressed character from keyboard or image.

In-out screen control unit: Controls whether in the desired screen area in Fig.2.

A detailed block diagram of VGA monitor controller is shown Fig. 3. In this block diagram, if column and row coordinates received from main VGA controller is in our screen area, it activates the our VGA monitor controller else deactivates. After activated, other units enable. When the output of column pixel pointer unit is 0x7, column pointer unit activates. In the same way, the work of other units depends on the output of units connected. The outputs received these units are calculated the related memory address. This address is used to store the bit map of pressed character.

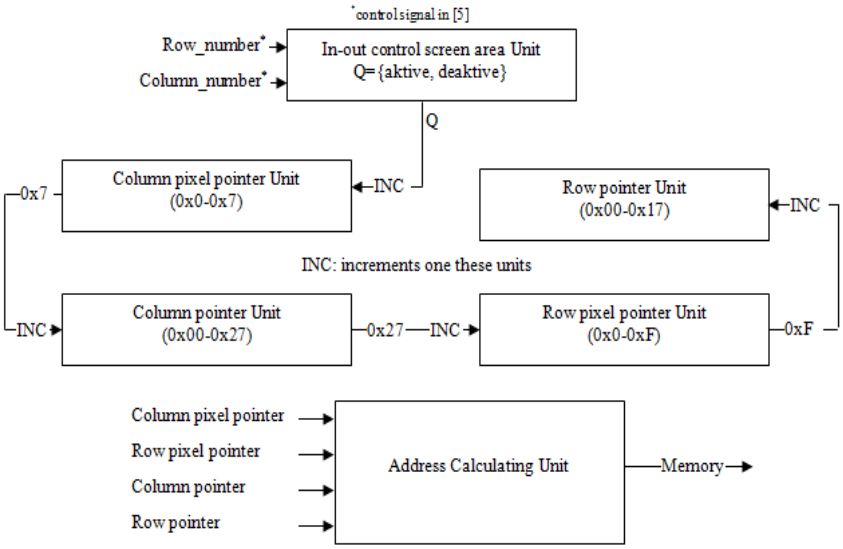

Fig.3 The block diagram of VGA monitor controller

It is occupied 4KB in the main memory for bit maps of characters from 0x9000 address. The bit map of every character should be taken from and placed to the related memory area according to following procedure.

Step-1: Start Procedure

Step-2: Take ASCII code of pressed key.

Step-3: If ASCII code=odd then go to Step-5

Step-4: Calculate address=0x9000+(ASCII code/2) and take bit map of character at most significant bits of memory(15-8.bits) in the calculated address and go to Step-6.

Step-5: Calculate address=0x9000+(ASCII code/2) and take bit map of character at least significant bits of memory(7-0.bits) in the calculated address.

Step-6: Storing process of bit map: Calculate address=

0xA000 + ((Row_pointer*40)+Column_pointer)/2)*16+Row_pixel_pointer Step-7: Scan continuously the related range of memory area (0xA000-0xAFFF).

Step-8: Finish procedure.(Note: Every word in the main memory is 16-bit length)

Since this controller has modular nature, it can be adopted the other architecture design using the following steps.

Step-1: If you change the desired area in display screen, the starting and finishing points should be defined. Then 2's complement of these points must be changed the old one in In-out control screen area unit.

Step-2: If you change the size of a character, the required changes, only the bit count of counter, must be made in Column pixel pointer unit and/or Row pixel pointer unit

Step-3: If you change the sizes of column and/or row, the bit count of counter in Column pointer unit and/or Row pointer unit must be changed.

4. Summaries

This article presented a modular approach to VGA monitor controller for BZK.SAU.FPGA10.1 microcomputer architecture design. FPGAs are currently the main implementation technology of digital systems. The possibility of reconfiguring the circuits allows the students to perform unlimited design iterations without additional costs. So the modular approach to VGA monitor controller was implemented on FPGAs development platforms in this article. The main benefits of the modular approach provide to both students and teachers as follows:

(1): The student can easily design any size of VGA monitor controller defined in section 3.

(2): S/he can discover the internal structures of the VGA monitor controller since it is available our website[10] at no cost.

(3): Using this controller, it is very simple to write assembly programs on BZK.SAU.FPGA10.1 microcomputer architecture design rather than writing machine code.

The proposed modular approach is beneficial to computer engineering, computer science, and electrical engineering students and to anyone who would like to gain an understanding of the hardware concepts of computers in general.

5. Acknowledgment

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