

## Simulation and Modeling of Capacitive Coupling Interconnection For 3D Integration

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**Abstract.** This study presents the simulation and modelling of a capacitive coupling interconnection circuit for three-dimensional (3D) system integration. The potential benefits of 3D integration provide an alternative to scaling when it comes to cramming more functionality in a smaller space. It could also enable an increase in performance by shortening signal paths. The proximity data link is performed via capacitive couplings between the top facing dies for 3D system integration. In the study, based on 3D electromagnetic (EM) simulations of High Frequency Structure Simulator (HFSS) for the capacitive pad between two pads of dies have been simulated. The simulation results show that the effect of cross-coupling between adjacent channels is dependence on substrate characteristic and pads arrangement. In addition, the HSPICE simulation results show that the data rate up to 2 gigabit per second (Gbps) can be achieve using TSMC 0.18 $\mu$ m 1P6M CMOS technology.

**Keywords:** Proximity data link, electromagnetic (EM), HSPICE, capacitive coupling

### 1. Introduction

More and more functionality has been integrated into single chips leading eventually to system-on-chip (SoC) implementations [1]. However, a SoC may not always be the optimum solution due to extensive die size, number of interconnects and problems with technology compatibility and migration. A comparison of 3D integration to SOC approaches shows SoC will take time and often require substantial resources but will eventually yield positive returns – at least for high-end or long-running applications. However, for other products having a relatively short life cycle, 3D die stacking or package stacking will have a decisive advantage in both time and economics. For a three-dimensional integrated circuit (3DIC)-implementation the difficulty of handling the increased amount of interconnects between separate chips arises. Traditional wire bonding methods suffer from poor area efficiency. As bonding pads are situated in the perimeter of the die, the integration density of wire bonding does not increase at the same rate with the complexity of a single chip. The use of solder bumps (flip-chip) provides a solution for the low density of traditional bond pads. However, this approach requires additional, and therefore costly, process steps. Also the achievable yield of the product is lower due to these extra manufacturing steps.

The feasibility of connections based on interconnects of capacitive coupling [2-10] has been reported by several papers. They studies can achieve high-bandwidth communication links with high integration density. This makes it possible to stack the chips thus leading to a smaller footprint. Also extra manufacturing steps can be avoided, if the communication between the chips is done using a wireless method. The capacitive interconnects two stacked chips is presented in Figure 1.

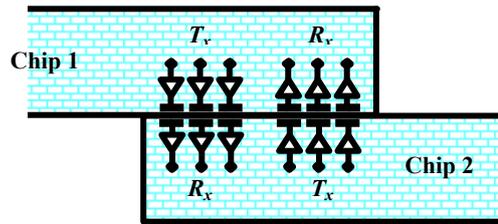


Figure 1. Cross-section of chip-to-chip capacitive interconnection.

Capacitive coupling interconnection is based on the observation that faster, lower-cost communication is possible over shorter distances. Placing the transmitter and receiver in extremely close proximity, with only microns of separation between them should therefore lower overall communication costs. This can be done by placing two chips face-to-face in a manner that aligns the transmitter circuits of one chip with the receiver circuits of the other. Only partially overlapping the two chips grants access to the rest of the chips' surfaces for power delivery [2]. The rest of the paper is organized as follows. Section 2 presents a brief description of the capacitive coupling interconnect mechanism and the coupling pad modelling. The simulation results of a capacitive coupling interconnection circuit are provided in Section 3. Finally, we conclude our paper in Section 4.

## 2. Capacitive Coupling Interconnects

### 2.1 Capacitance Effects

Any two objects that are capable of being electrically charged and which are separated by some dielectric material will form a capacitor. This relationship is described mathematically in Equation (1), where  $Q$  is the charge (measured in Coulombs),  $C$  is the capacitance (Farads), and  $V$  is the voltage (Volts). Larger capacitances lead to greater accumulation of charge for a given voltage difference. [11]

$$Q = CV \text{ [Coulombs]} \quad (1)$$

Capacitance can be produced between objects of any shape. The capacitances of concern in this project occur between coupling pads which, as we shall see, can be fairly accurately modelled as parallel-plate capacitors. For parallel-plate capacitors, the capacitance is given,

$$C = \epsilon \frac{WL}{d} \text{ [Farads]} \quad (3)$$

where  $W$  is the width of the parallel plates (meters),  $L$  is the length of the plates (meters),  $d$  is the distance between the plates (meters), and  $\epsilon = \epsilon_0 \cdot \epsilon_r$  (Farads/meter) where  $\epsilon_0$  is the permittivity of free space ( $8.854 \cdot 10^{-6}$  pF/m) and  $\epsilon_r$  is the relative dielectric constant of the material between the plates[11].

The main problem in capacitive interconnects is the need for accurate alignment between the chips [8]. Misalignment leads to weaker links and larger cross-talk between the adjacent channels, thus increasing the bit error rate (BER). Sensitivity to alignment mismatch can be decreased by increasing the size of the capacitor plates, but those results in smaller integration density. The other approach is to use an electronic alignment correction technique [9], in which the capacitors are divided to a large number of smaller capacitors. The data in the transmitting channel is switched to those capacitors that are best aligned with the receiver side.

The values of the link capacitances are small, in the order of femtofarads (fF), due to a large separation distance between the plates compared to their area. This large distance also leads to larger fringe capacitance in relation to the link capacitance. In designing a capacitive interconnects system; the problem of correctly modelling the link capacitance arises. As other circuit components have an electrical model, it would be beneficial if the interconnects themselves would also have a circuit representation. Since the capacitor plate dimensions are on the same scale as their distance, separate EM-simulators are needed to accurately model the link. The output data of these simulators is usually in form of S-parameters. The following section describes a method of acquiring a lumped circuit model representation from the S-parameter data of an EM-simulator.

### 2.2 Coupling Pad Modelling

The following approach to create the link model has been undertaken. First, a substrate definition has been created in HFSS software, reflecting the substrate, metallization, vias and oxide layers of the CMOS stack. The physical dimensions (e.g., a thickness of each layer) and parameters (e.g., contact resistances, permittivity of isolation materials) have been chosen according to the fabrication process documentation. The process used was a  $0.18 \mu\text{m}$  1P6M standard CMOS process. A mirrored (vertically flipped) copy of this stack has been placed above, creating a flip-chip arrangement with an air gap between the chips. Then, a layout for two adjacent channel data-link-couplings has been drawn. The link-coupling structures in both chips included a connection for the top metal layer. The plate size could be enlarged to  $100\mu\text{m} \times 100\mu\text{m}$  without sacrificing the underlying layout density. The resulting structure is sketched in Figure 2.



Figure 2. Structure representing coupling channels in top-faced CMOS stacks for (a) parallel type and (b) butterfly difference type.

When the 4-port structure representing two adjacent capacitive coupling interconnection channels was ready, a set of 3D full-wave electromagnetic field simulations has been performed using High Frequency Structure Simulation (HFSS) full wave solver from Ansoft to consider the silicon substrate loss of coupling chip. The system was analysed for a frequency range of 1GHz to 10GHz with adjacent channel space of  $2 \mu\text{m}$  and chips gap value of  $4 \mu\text{m}$ . An example of S-parameters simulation results is shown in Figure 3, in which a signal transfer of a data-link-coupling and cross-coupling are plotted versus frequency. The obtained sets of S-parameters were converted into Z-parameters, which later were used for the extraction of component values in the lumped circuit model.

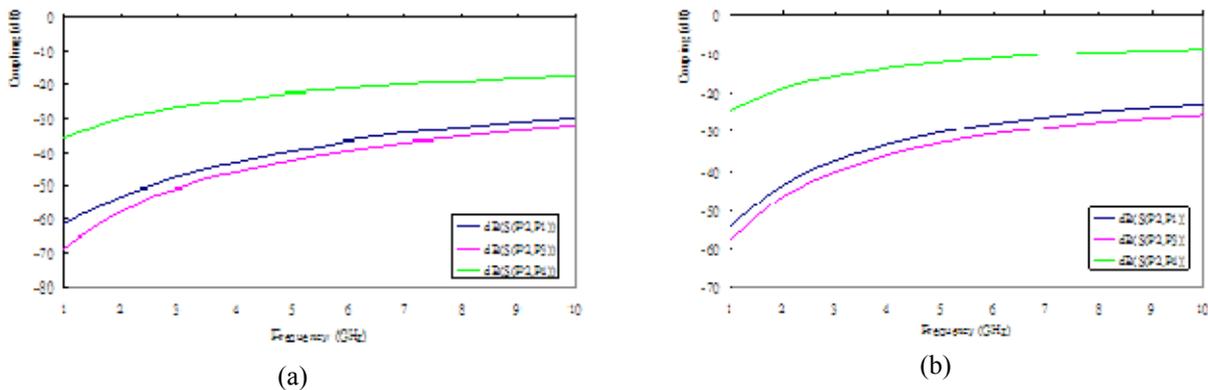


Figure 3. Example of S-parameters simulation results for (a) parallel difference type and (b) butterfly difference type.

The frequency response of varying substrate for a  $100 \mu\text{m}$  diameter coupling pad with separation  $4 \mu\text{m}$  is shown in Figure 4 and 5. Figure 6 show the difference size of the transfer coupling simulation resulting. The data-link coupling is quite dependent of the pads size.

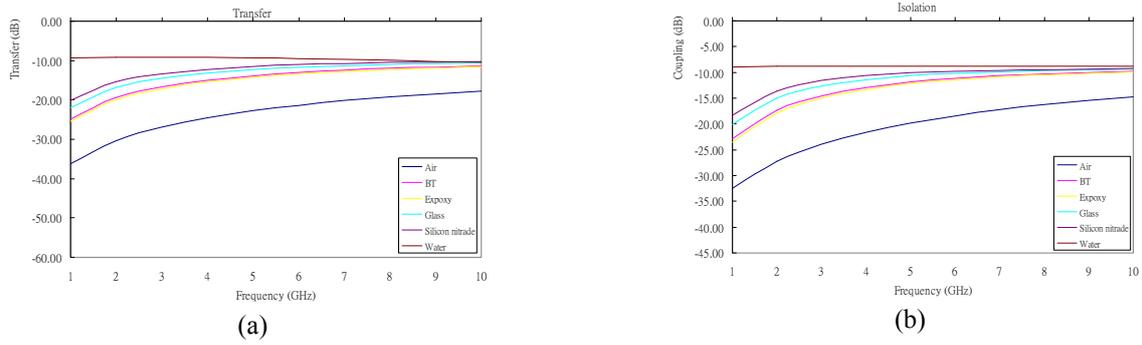


Figure 4. The comparison of the S-parameters simulation resulting for parallel type substrate.

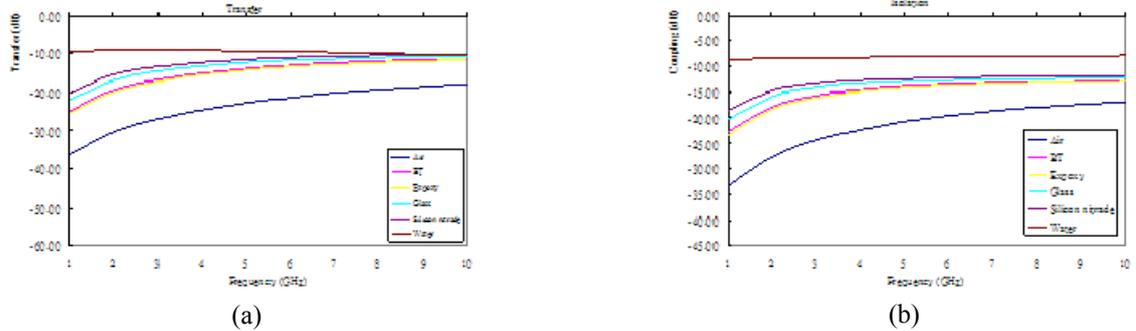


Figure 5. The comparison of the S-parameters simulation resulting for difference type substrate.

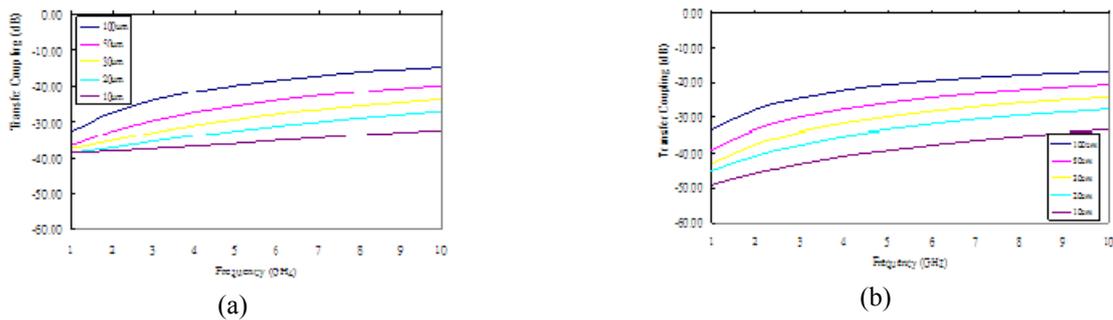


Figure 6. The difference size of the transfer coupling simulation resulting for parallel type (a) and butterfly difference type (b).

### 3. Coupling Interconnect Circuit Simulation

In designing a capacitive interconnection system; the problem of correctly modelling the link capacitance arises. As other circuit components have an electrical model, it would be beneficial if the interconnections themselves would also have a circuit representation. The transmission circuit is buffered by an inverter. The receiver inverter is connected through a feedback loop for signal amplification at the receiving end Rx. Then, another two inverters are designed at the rear tandem O1 for signal integrity and to restore full signal amplification. Figure 7 shows the circuit diagram.

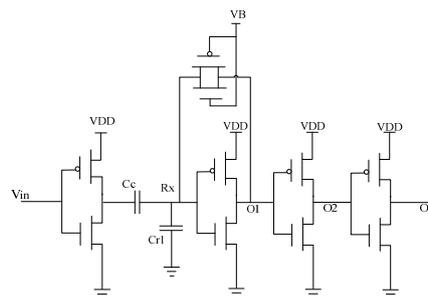


Fig. 7 Transmission circuit of capacitive coupling.

The inverter and feedback inverter at the receiving end can be used to control the effect of the signal amplification. HSPICE simulations are performed to observe the effects of capacitive coupling interconnection. The simulation is based on TSMC 0.18  $\mu\text{m}$  library. The input signal through Tx and the coupling capacitor transmitted to the Rx and recover back to its original signals. The simulation results at different nodes to show the waveform are shown in Figure 8.



Fig. 8 HSPICE simulation results for capacitive coupling interconnection.

The eye diagram provides visual information that can be useful in the evaluation of system performance and can offer insight into the nature of channel imperfections. The simulated eye diagram shown in Figure 9 indicates the signal transmission quality is good for the present capacitive coupling circuit at 2 GHz operation region.

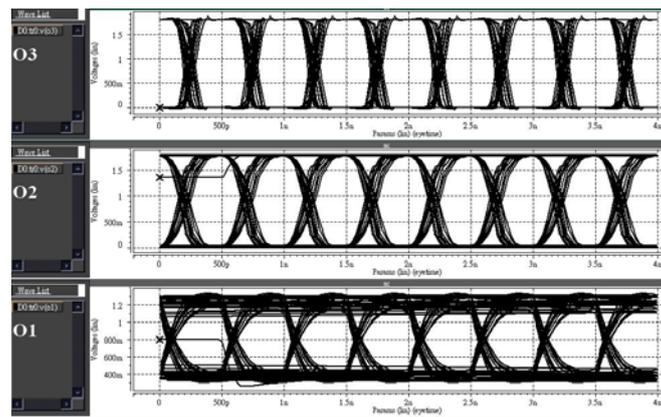


Fig. 9 Simulated eye diagram waveform.

## 4. Conclusions

The simulation and modelling for a capacitive coupling interconnection is demonstrated using HFSS and HSPICE simulation tool. It provides an understanding of how the physical parameters affect the design. The S-parameter simulation results show the butterfly difference signal type is good for parallel difference signal type. This leads to optimal sizing of the link capacitors and the design of transmitter/receiver. The HSPICE simulation results indicate the capacitive coupling interconnection for TSMC 0.18 $\mu\text{m}$  1p6M process can operate up to 2 GHz.

## 5. Acknowledgments

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