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Simulation and Control of Binary Distillation Column Using XMOS Technology

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Abstract. In the present work the mathematical model of binary distillation column is simulated with the help of MATLAB. Different parameters of distillation column are analyzed. A PI controller is designed to control the quality of distillate. The same mathematical model of binary distillation column is implemented on VLSI (XMOS) technology to have better response of the process. This is the most advanced technology in the field of VLSI and has better features as compared to the conventional techniques. The simulation results obtained through XMOS technology are compared with the simulation results obtained from MATLAB. The execution time of both the techniques are compared and found that XMOS technology took less time as compared to MATLAB.

Keywords: distillation, process control, PI controller, VLSI, XMOS technology

1. Introduction

Distillation is a process of separating mixtures based on differences in their volatilities in a boiling liquid mixture. Distillation process may be classified in two categories namely binary distillation and multicomponent distillation. The objective of analysis of mathematical model is to develop a robust and efficient control technique for binary distillation column. The model is constructed based on the physical properties of the system, such as the preservation of mass, energy and momentum. The mathematical models range from simple to rigorous models depending on the levels of complexity and the assumptions.

The quality of the product may be curbed by different control techniques and the controllers to curb the process may be conventional, intelligent and inferential type. In the present work a PI controller is designed and used to control the quality of distillate. A conventional controller has proportional–integral–derivative controller (PID controller) in a generic control loop feedback mechanism. A PID controller calculates an "error" value as the difference between a measured process variable and a desired set point. The controller attempts to minimize the error by adjusting the process control inputs. The PID parameters used in the calculation must be tuned according to the nature of the system. The response of the controller can be described in terms of the desired parameters of the controller to an error.

$$C(S) = K_P + \frac{K_i}{S} + K_D S \tag{1}$$

$$C(S) = K_P(1 + \frac{1}{T_i S} + T_D S) \tag{2}$$

Where K_P = Proportional Gain

K_i= Integral Gain, Ti = Reset Time

K_D=Derivative gain, T_D= derivative time

By tuning all the three constants (KP, Ti and TD) in PID controller algorithm, the controller takes action designed for specific process requirements. In the present work a PI controller is designed and tuned with the

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help of Ziegler-Nichols chart. The designed PI controller is then used to control the distillate quality of the product.

The rest of the paper is arranged in the following sections. The section 2 presents mathematical model of Binary Distillation column. The simulation results are discussed and shown in section 3. The XMOS technology is briefed in section 4, with its features and hardware description. In section 5 the simulated results using XMOS technology and MATLAB are compared. The final concluding remarks are detailed in section 6.

2. Mathematical Modeling

In order to represent realistic operation of actual distillation process, a rigorous nonlinear model that considers simultaneous effect of heat and mass transfer operations and fluid flow on the plates is needed. Such distillation model is derived from the principles involving dynamic material and component, and algebraic energy equations supported by vapor liquid equilibrium and physical properties. An automated system is used to maintain the output within desirable limits by means of a control action.

The following assumptions have been made to simplify the mathematical model of binary distillation column. The simulation program is developed for binary distillation column based on these assumptions:

- Staged batch distillation column with trays numbered from the bottom to top.
- Perfect mixing and equilibrium on all trays.
- Constant stage pressures (atmospheric) and tray efficiencies.
- Negligible tray vapors holdups.
- Total condensation with no sub cooling in the condenser.
- Variable liquid holdup on each tray.
- Vapour flow rate is constant.
- Constant liquid holdup in the reflux drum.
- Raoult's law for the vapour–liquid equilibrium.

The molar holdup on nth tray is given by the following equation:

$$\frac{dM_n}{dt} = L_{n+1} - L_n \tag{3}$$

where

L_{n+1}= Liquid flow rate coming to n^{th} tray, lb-mole/hr

L_n =Liquid flow rate leaving n^{th} tray, lb-mole/hr

The material component balance on n^{th} tray is given by the equation as follows.

$$\frac{dM_n x_n}{dt} = L_{n+1}x_{n+1} + Vy_{n-1} - L_n x_n - Vy_n \tag{4}$$

where

V = Vapor flow rate, lb-mole/hr

y_n = vapor composition on nth tray, mole fraction

The vapor composition and liquid flow rate on n^{th} tray is given by the following equations.

$$y_n = \frac{\alpha x_n}{1+(\alpha-1)x_n} \tag{5}$$

$$L_n = L_n + \frac{(M_n - M_{n-1})}{\beta} \tag{6}$$

where

x_n = Liquid composition on n^{th} tray, mole fraction

M_n = Liquid Molar hold up on n^{th} tray, lb-mole

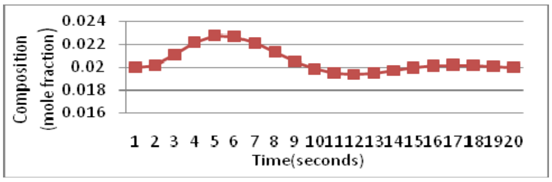
L_n = Liquid flow rate from n^{th} tray, lb-mole/hr

β = Hydraulic time constant

As stated earlier also that PI controller is used to control the quality of the output product, therefore the PI controller is designed to improve the performance of the process using MATLAB, and the same is designed using XC language on software XMOS development tools.

3. Simulation Results

The mathematical model of binary distillation column is simulated with all assumptions involved and various parameters of the column are observed with time. The variation of different output variables with time are shown from Fig.1 to Fig.5.



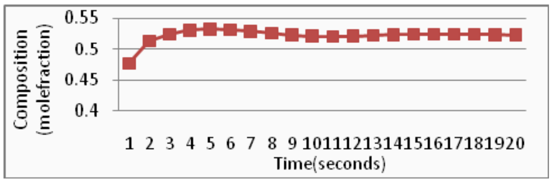
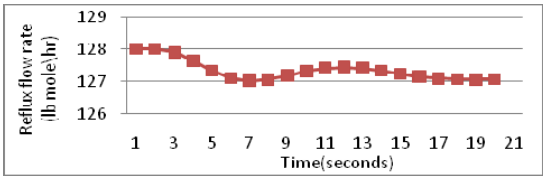


Fig. 1: Bottom Product composition (X_B) with time

Fig. 2: Distillate product composition (X_D) with time



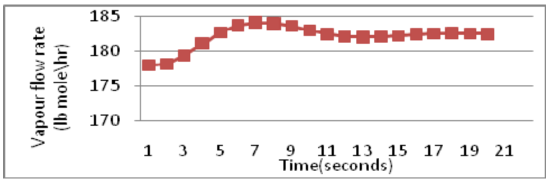


Fig. 3: Reflux flow rate(R) with time

Fig. 4: Vapour flow rate (V) with time

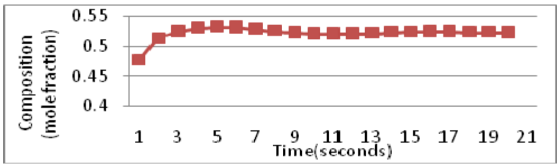


Fig. 5: Composition on tray-10(X_{10}) with time

The simulated results of bottom product composition, distillate composition, vapour flow rate from reboiler, reflux flow rate and liquid composition on 10^{th} tray with time are shown in Fig. 1, Fig. 2, Fig. 3, Fig. 4 and Fig. 5 respectively. It is observed from Fig. 1 to Fig. 5 that all the output variables are approaching steady state position on or after 9.5 seconds. The same model may also be simulated using digital techniques for better control and analysis purpose. Among the various other digital techniques the XMOS is found to be the most suitable one. The binary distillation column is therefore implemented on XMOS hardware kit, to achieve better efficiency of the process and after simulation on hardware kit the simulated model can be interfaced with the real world process easily for control and analysis purpose. A brief introduction of XMOS technology is given in next section.

4. XMOS Technology

XMOS has several advantages over FPGA; most importantly it is a multicore processor resulting in the best possible mix of solutions of flexibility, price and performance. The XMOS XS1-L family of devices are based on the XMOS Xcore processor, a 500 MIPS(Microprocessor Without Interlocked Pipeline Stages) event-driven RISC(Reduced Instruction Set Computer) processor with 100% deterministic operation, a 32x32 multiplier, programmable I/O and a host of other resources, all programmable entirely in C++, C and XC. XC includes extensions to C for concurrency, communications, and timed I/O operations. XMOS devices can be used as a direct substitute for low cost SRAM (Static Random Access Memory) based FPGAs (Field Programmable Gate Arrays). A single core XS1-L device offers a capacity for general digital logic implementation roughly comparable to an FPGA having 7-20K logic elements (roughly 70K-200K ASIC gates). The XMOS architecture is explained in the following section.

4.1 XMOS architecture:

It enables systems to be constructed from multiple Xcore processors connected by communication links. Every XMOS device includes one or more Xcores and a high speed low latency switch. The switches are used to route messages between Xcores and chips, and between chips, via the links. The different parts of XMOS processor are explained in the following section and shown in Fig. 6.

4.2XCORE processor: The Xcore is a multithreaded processing component with instruction set support for communication, I/O and the time taken to execute a sequence of instructions can be accurately predicted. This makes it possible for software executing on an Xcore to perform many functions normally performed by hardware, especially DSP and I/O. Instead of writing code in HDL, in XMOS technology the codes are written in C, C++ or XC to implement deterministic processing functions, which is easier with respect to HDL. The XMOS has some distinct features which are described in the next section.

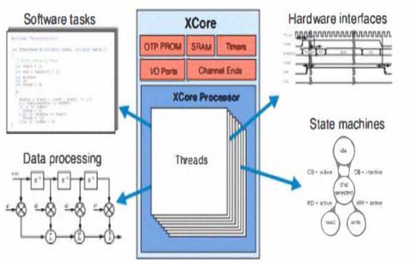


Fig. 6: Architecture of XMOS

4.3 Unique features of XMOS: The distinct features of XMOS used for simulation of the model are as follows:

4.3.1 Parallelism

An Xcore processor runs multiple real-time hardware threads simultaneously. Each thread has access to a dedicated set of general purpose registers. It gets a guaranteed share of the processing power, and executes a program using common RISC-style instructions. Each thread can execute simple computational code, DSP code, control software (taking logic decisions, or executing a state machine). It can also handle I/O operations using intelligent I/O resources. The eight hardware threads, generous MIPS, 100% deterministic architecture and intelligent I/O provide designers with the flexibility of HDL. This leads to easing the design entry and verification tasks.

4.3.2 Threads, memory and channels

Threads can be used as channels to provide buffered, event-based communication between threads. It allows data exchange and synchronization using single cycle instructions. Alternatively, threads can share 64KB of on-chip SRAM memory to exchange data, using single cycle lock instructions to co-ordinate access. This makes the implementation of lightweight protocol stacks (such as TCP/IP) that fit within the 64KB of memory essentially free when compared to an equivalent implementation in an FPGA. This requires a soft core such as Xilinx's MicroBlaze and an external memory interface that would consume a large portion of the FPGA capacity, not to mention adding an external memory chip to the bill of material cost.

4.3.4 Simulation results

The parameters simulated from MATLAB program are also obtained using XMOS simulation program. The graphical plot for bottom product composition and distillate product composition with time are shown in Fig. 7 and Fig. 8 respectively. It is observed from Fig. 7 and Fig. 8 that the simulated results obtained from XMOS technology are matching with the results obtained from simulation program using MATLAB. The graphical plot for liquid composition on 10^{th} tray is shown in Fig. 9. It is observed from Fig. 9 that the simulated results obtained from XMOS technology are coinciding with the results obtained from MATLAB. The same observations are made for the vapor flow rate, and reflux flow rate. The Graphical plot for vapor flow rate and reflux flow rate are shown in Fig. 10 and Fig. 11 respectively.

Simulation of binary distillation column on XMOS have proved to be a better simulating tool as XMOS has taken only 1.73 microseconds whereas MATLAB took 0.225199 seconds in execution. Therefore it can be concluded that using XMOS technology, a process may be controlled much before than the control action is being taken by MATLAB simulation program, in case of any disturbance. The developed simulation program using XMOS technology is realized with the help of XK-1 hardware kit and the real time distillation process may be controlled with the help of the above mentioned hardware kit.

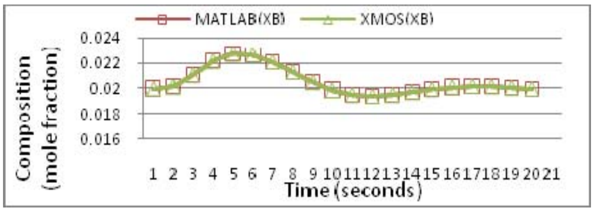


Fig. 7: Bottom product composition with time

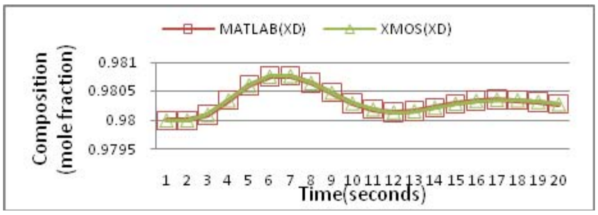


Fig. 8: Distillate product composition with time

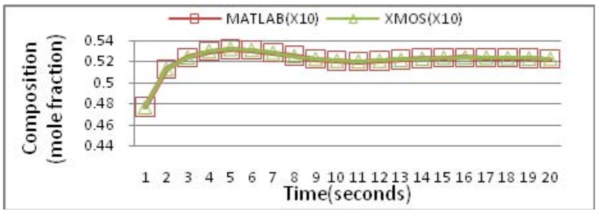


Fig. 9: Liquid Composition on 10th tray with time

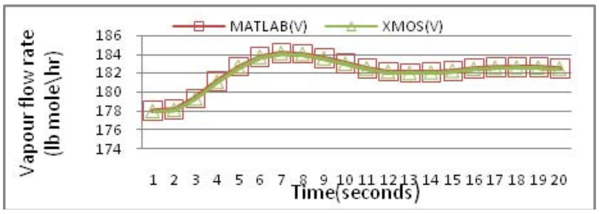


Fig. 10: Vapour flow rate with time

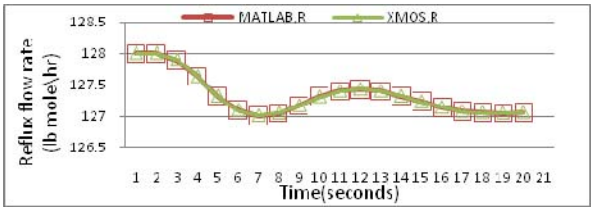


Fig. 11: Reflux flow rate with time

5. Conclusion

In the present work the mathematical model of binary distillation column is simulated with the help of MATLAB. A PI controller is designed to control the quality of product at specified level. The same mathematical model of binary distillation column is simulated with the help of XMOS technology including PI controller design. This is the first effort to simulate the model of binary distillation column on the hardware (XMOS kit). With this approach it is concluded that XMOS has better controlling capabilities than other technologies i.e. MATLAB and C++ in terms of execution time. The XMOS is an advanced version of Xilinx and have very unique and different features from Xilinx. A new printed circuit board is being designed using XMOS chip with a hope that resulting PCB will be of less cost and same binary simulation program will be implemented on it and expecting the same results as on the original XMOS kit.

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