

# Novel Stochastic Inductance Model of CMOS Monolithic Active Inductor

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**Abstract.** In this research, a novel model that describes the stochastic effect of supply noise to the inductance of the CMOS monolithic active inductor has been proposed. Unlike the previous model, the Gaussian stochastic process with white power spectral density has been adopted in order to model the distribution of noise. Furthermore, the  $N^{\text{th}}$  order approximation of the stochastic process has also been used. So, the proposed model has been found to be more realistic than the previous one. This model can accurately capture the stochastic behavior of the resulting inductance obtained from the Monte-Carlo SPICE simulation of the candidate sub 100 nm CMOS monolithic active inductor with a confidence level as high as 99%. Hence, it has been found to be a convenient tool for the precision analysis along with the high accuracy aimed design of various active inductor based applications.

**Keywords:** CMOS monolithic active inductor, Gaussian stochastic process,  $N^{\text{th}}$  order approximation, Stochastic model

## 1. Introduction

CMOS monolithic active inductors have been found to be applicable in many analog and mixed signal circuits, for example filters, oscillators and many signal processing/communication circuits. The examples of these active inductors have been proposed in [1-3]. The resulting inductance has been found to be dependent upon the DC transconductance ( $g_{m0}$ ) of the basis transistor. Such  $g_{m0}$  is the function of the bias current which can be drawn from the supply. Theoretically, the accurate tuning of the inductance value which yields a constant inductance value at the desired one, can always be obtained since the bias current is always constant at the selected value.

Practically, the supply is suffered by noise, so the drawn bias current is corrupted by such noise. Hence, the bias current has become a stochastic process. It is randomly varying as time goes by, no longer be constant at the selected value. By this stochastic nature of the bias current, the resulting inductance also become a stochastic process, no longer be a constant value at the desired one. This means that accurate tuning cannot be achieved. This is a catastrophic situation for the design of all applications, particularly those with high precision requirements since the desired performance cannot be guaranteed.

Previously, the stochastic model for the resulting inductance of the CMOS monolithic active inductor has been proposed in [4]. The proposed model in this study has been derived based on the assumption that the bias current is uniformly distributed. This is practically not the case since noise is typically modeled with Gaussian stochastic process with white power spectral density. Furthermore, this model has been derived based upon a first order approximation of the stochastic process [5], which is equivalent to the estimation of the whole process by using the data obtained from only one instance of observation. So, it is practically invalid. A more realistic model is desired.

Hence, the stochastic model which captures the effect of supply noise to the inductance of the CMOS monolithic active inductor has been proposed in this research. Unlike [4], the Gaussian stochastic process with white power spectral density has been adopted in order to model such noise. Furthermore, the  $N^{\text{th}}$  order approximation [5], which is equivalent to the estimation of the process by using the data obtained from  $N$

instances of observation, has also been used. Hence, the proposed model has been found to be more realistic than the previous one. This model is highly capable of capturing the stochastic behaviour of the resulting inductance obtained from the Monte-Carlo SPICE simulation of the candidate sub 100 nm CMOS monolithic active inductor with a sufficiently high confidence level given by 99% due to the corresponding K-S test result. Hence, the proposed model has been found to be a convenient tool for the precision analysis along with the high accuracy aimed design of various applications involving CMOS monolithic active inductor particularly those which their performances can be significantly degraded by the supply noise for example voltage controlled oscillator, phase locked loop, PRBS generator and high speed serial link transmitter.

## 2. The Proposed Model

In this section, the proposed model will be presented by starting with its derivation. Similarly to [4], the resulting inductance of the CMOS monolithic active inductor can be given by

$$L = \frac{C_{gs}}{g_{m0}^2} \quad (1)$$

where  $C_{gs}$  denotes the gate-source capacitance and  $g_{m0}$  can be written as a function of the bias current ( $I_B$ ) of the basis transistor as  $g_{m0} = \sqrt{\beta \cdot I_B}$ . Note that  $\beta$  denotes the current factor which can be given by  $\mu_n C_{ox}(W/\lambda)_n$  and  $\mu_p C_{ox}(W/\lambda)_p$  for the CMOS monolithic active inductors with NMOS based core and those with PMOS based core, respectively. Also similarly to [4],  $\lambda$  is used to denote the channel length to avoid confusion

Since  $I_B$  is practically corrupted by the supply noise, it become a stochastic process denoted by  $I_B(t) = I_B + n(t)$  where  $n(t)$  denotes noise in the biasing caused by using the noisy supply. Of course,  $n(t)$  is a Gaussian stochastic process with white power spectral density and the resulting inductance also become a stochastic process given by

$$L(t) = \frac{C_{gs}}{\beta[I_B + n(t)]} \quad (2)$$

With  $N^{\text{th}}$  order approximation [5], the PDF of  $n(t)$  can be given by

$$f_n(n(t), t; n(t+\tau), t+\tau, \dots; n(t+(N-1)\tau), t+(N-1)\tau) = \prod_{i=0}^{N-1} \left\{ \frac{1}{\sqrt{2\pi}N_{rms}} \exp\left[-\frac{(n(t+i\tau))^2}{2N_{rms}^2}\right] \right\} \quad (3)$$

where  $n(t+i\tau)$  is  $n(t)$  at any  $i^{\text{th}}$  instant and  $N_{rms}$  denotes the root mean square value of noise.

As  $L(t)$  is a function of  $n(t)$ , It is approximately a Gaussian stochastic process as well. Since  $n(t)$  is a zero mean stochastic process, mean value of  $L(t)$  denoted by  $L(t+i\tau)$  can be simply found as follows

$$\overline{L(t+i\tau)} = \frac{C_{gs}}{\beta I_B} \quad (4)$$

On the other hand, the standard deviation of  $L(t)$  denoted by  $\sigma_L(t+i\tau)$  can be given in terms of  $N_{rms}$  as

$$\sigma_L(t+i\tau) = \frac{C_{gs} N_{rms}}{\beta I_B^2} \quad (5)$$

Hence, the proposed model is now derived as follows

$$f_L(l(t), t; l(t+\tau), t+\tau, \dots; l(t+(N-1)\tau), t+(N-1)\tau) = \prod_{i=0}^{N-1} \left\{ \frac{\beta I_B}{\sqrt{2\pi} C_{gs} N_{rms}} \exp\left[-\frac{(l(t+i\tau) - \frac{C_{gs}}{\beta I_B})^2}{2 \left[\frac{C_{gs} N_{rms}}{\beta I_B^2}\right]^2}\right] \right\} \quad (6)$$

where  $l(t+i\tau)$  denotes the sampled value of the inductance at any  $i^{\text{th}}$  instant.

This model is more realistic than that in [4] since the Gaussian distribution of  $n(t)$  and the  $N^{\text{th}}$  order approximation have been adopted. Of course, much of the stochastic information of the inductance value, for example mean, standard deviation and variance can be found analytically by using the proposed model. This

is the major contribution of this model to the design of various applications involving the CMOS monolithic active inductor in order to find the optimum design strategy. It can be seen by using the proposed model that the stochastic properties of the resulting inductance such as mean, variance and mean square are time invariant. So,  $L(t)$  is a stationary process which make it possible to be completely verified by using a single instant basis as will be shown in the subsequent section. The obtained result from just a single instant has been found to be stochastically valid for the entire process since the stochastic properties of the resulting inductance values have been found to be time invariant as formerly mentioned. Furthermore, it can also be found by using the proposed model that  $L(t)$  is not white even though  $n(t)$  is.

### 3. The Model Verification

The verification of the proposed model can be performed by comparing the distribution obtained from the parameterized model at an observed single instant to its counterpart obtained by performing the Monte-Carlo SPICE simulation of the candidate CMOS monolithic active inductor circuit. In this research, a simple CMOS monolithic active inductor that is also used in [4], is adopted as a candidate active inductor. Including the simplest possible biasing circuitry, this candidate CMOS monolithic active inductor circuit can be depicted as follows

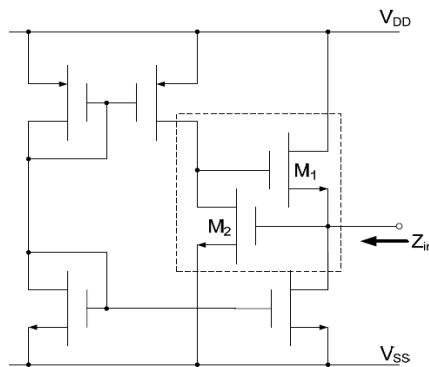


Fig. 1: Candidate CMOS monolithic active inductor which also used in [8].

The N-type based core active inductor circuit, composed of  $M_1$  and  $M_2$ , is enclosed in a broken line square. Based on the IBM 90nm RF CMOS parameters extracted by MOSIS, the distribution obtained from the model and that obtained from 2000 runs of the Monte-Carlo SPICE simulation of the candidate active inductor can be comparatively plotted in Fig. 2 which its x-axis has been normalized in term of the percentage of fluctuation in the inductance value from the desired one. It can be observed that a strong agreement between the parameterized model and the Monte-Carlo SPICE based counterpart exists. So, it can be seen that the proposed model has high capability to predict the stochastic behavior of the resulting inductance value according to the cited observed agreement.

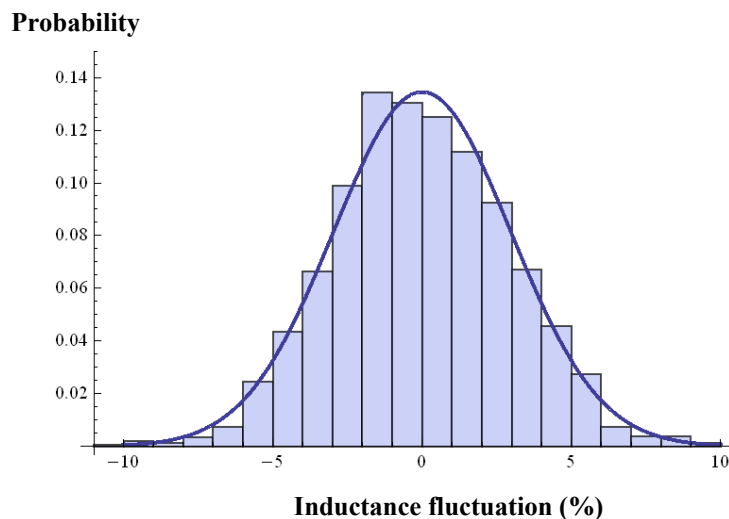


Fig.2: Model based distribution (line) v.s. Candidate circuit based one (histogram)

Furthermore, the goodness of fit test of the model is also performed via the K-S test, as mentioned above. By applying the K-S test methodology defined in [6] to the obtained distributions, the resulting K-S statistic can be found as  $KS = 0.03459$ . Let the confidence level of the test be 99%. In other words, let  $\alpha = 0.01$ . As the number of runs is 2000, the critical value of the test denoted by  $c$  can be found according to the formula proposed in [7] as  $c = 0.036448$ . As  $KS = 0.03459 < c = 0.036448$ , the model can fit the obtained data with 99% confidence. At this point, the accuracy of the model is now verified by the agreement seen in the comparative plots and the satisfactory K-S test result. This verification result is valid for the entire process due to the aforementioned reason.

#### 4. Conclusion

In this research, the stochastic model which captures the effect of the supply noise to the resulting inductance of the CMOS monolithic active inductor has been proposed. This model has been found to be more realistic than the previous one in [4], according to the usage of Gaussian distribution of noise and  $N^{\text{th}}$  order approximation of stochastic process. The proposed model can accurately capture the cited behavior with 99% confidence. This can be seen from the agreement between the model based distribution and that obtained from the Monte-Carlo SPICE analysis of the candidate sub 100 nm CMOS monolithic active inductor, along with a satisfactory K-S test result. The proposed model contributes a great deal of convenience to the analysis and design of any CMOS monolithic active inductor based application for example, the automatic tuning scheme for minimizing such inductance fluctuation can be implemented by using the proposed model as the mathematical basis.

Apart from the supply noise, the process variation induces the resulting inductance fluctuation as well. The modeling of such fluctuation can be simply performed by applying the available process variation induced MOS circuit level parameter models such as that proposed in [8]. If the state of the art CMOS technology in the nanometer regime is focused, the models for such nanometer CMOS technology for example, those in [9] and [10] have been found to be applicable.

#### 5. Acknowledgement

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#### 6. References

- [1] M. Ismail, R. Wassenaar, W. Morrison. A high-speed continuous-time bandpass VHF filter in MOS technology. Proc. IEEE International Symposium on Circuits and Systems. 1991, pp 1761-1764.
- [2] A. Thanachayanon, A. Payne. VHF CMOS integrated active inductor, Electron. Lett. 1996, 32: 999-1000.
- [3] A. Thanachayanon. CMOS floating active inductor and its applications to bandpass filter and oscillator design. IEE Proc. Circ. Dev. Syst., 2000, 147: 42-48.
- [4] R. Banchuin, R. Chiricharoen. The Stochastic based model of monolithic active inductor. Proc. International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology. 2010, pp.1-5.
- [5] A.H. Haddad. Probabilistic Systems and Random Signals. Prentice Hall, 2006
- [6] T. Altiok, B. Melamed. Simulation Modeling and Analysis with ARENA. Academic Press, 2007
- [7] S.A. Klugman, H.H. Panjer, G.E. Willmot. Loss Models: From Data to Decisions. John Wiley and Sons, 2008
- [8] H. Masuda, T. Kida, S. Ohkawa. Comprehensive matching characterization of analog CMOS circuits., IEICE Trans. Fundamental. 2009, E92-A(4): 966-975.
- [9] R. Banchuin. Process Induced Random Variation Models of Nanoscale MOS Performance: Efficient tool for the nanoscale regime analog/mixed signal CMOS statistical/variability aware design. Proc. 2011 International Conference on Information and Electronics Engineering. 2011, pp. 6-12.
- [10] R. Banchuin. Complete Circuit Level Random Variation Models of Nanoscale MOS Performance. Intl. J. Information and Electronic Engineering. 2011, 1(1): 9-15.