2009 International Conference on Computer Engineering and Applications
IPCSIT vol.2 (2011) © (2011) IACSIT Press, Singapore

A New Method for Designing QCA Circuits

Amir Khademhoseini, Abbas Vafaei

Department of Computer Engineering, Faculty of Engineering, Isfahan University
Isfahan, Iran

Abstract. In this paper we tried to solve some of the problems in logical designing based on Quantum-dot Cellular Automata (QCA) technology especially by using Null Convention Logic (NCL) instead of traditional Boolean logic and design circuits by using Locally Synchronous Globally Asynchronous (LSGA) method, and solve the problem of using feedback inside the QCA gates in this method, by design the gates that haven't any feedback. By this proposed method and designed gates we can design and build logical circuits based on QCA technology that may have fewer error rates.

Keywords: QCA; LSGA; NCL

1. Introduction

After introducing QCA technology as a possible substitution for CMOS technology, a great number of researches have been conducted to find out different dimensions of the QCA technology, its week points and its advantages. The purposes of all these studies have been removing the problems and shortcomings of this technology to be able to use it practically. One of the fundamental problems of this technology, the timing of circuit is highly dependent on the arrangement of the elements of the circuit. This rigorous dependency cause differences between the well-known trends of designing based on CMOS and designing based on QCA so that it seem we need new methods to have logical designs based on QCA. One of the proposed methods is designed the small parts of the circuit synchronously and connecting them together asynchronously. This method have solved some of the designing problems, however, it has its own problems. In this article, it's tried to propose a new way of solving one of these problems.

2. QCA Basics

Because of its very small nature (the possibility of being built in molecular Even atom level) and also its ultralow power consumption QCA has received a lot of consideration. A QCA cell as shown in Fig. 1 is considered as a square with four dot as its corners. The cell is loaded with two extra electrons (free electrons), which can quantum mechanically tunnel between cell dots but cannot tunnel between cells.

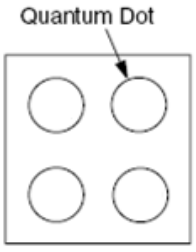

Fig. 1

With the placement of these two extra electrons in the four dots and due to the electrostatic repulsion, the two free electrons only can be at two stable positions. These two conditions considered as -1 and +1 polarity or Boolean values 0 and 1 respectively [1]. Fig. 2 shows these conditions. One of the main discussions of QCA is the intercellular movement of electrons. As it was maintained, the two free electrons of each cell can only be in two stable conditions. The movement of each cell free electrons between its dots is done through

tunneling mechanism. There are some barriers among adjacent dots in each QCA cell (inter-dot barriers) whose control can lead to a control of the free electrons and hence control the polarity of each QCA cell. In QCA, the control cycle is divided into the following four phase: Switch, hold, release and relax. During the switch phase, the inter-dot barriers of QCA being going up and make the electrons which were moving easily, fixed and stable. During the holding phase, as a result of the inter-dot barriers held high, the electrons keep their status and cannot move between cell dots. During the release and relax phases, the barriers come down and hence, the electrons can freely move within their cells. During the holding phase, cells are in one of two stable positions (-1 or +1 polarity), but in the release and relax phase electrons don't have a fixed position. Clocking mechanism is tool that control inter-dot barriers in QCA [2]. Generally speaking, when the cell is in the switch phase, it is under the influence of its adjacent cell which is in the hold (or switch) phase, and according to the arrangement of the cells, adopts the polarity of adjacent cell.

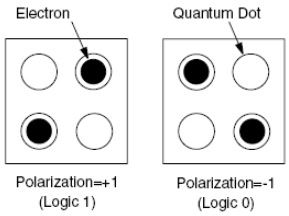

Fig. 2

By arrange QCA cell in proper arrangements it's possible to transfer binary information even build logical elements.

Two different kinds of arrangements are used to put QCA cells beside each other and transfer binary information. Which are shown in Fig. 3. The majority voter gate can be built as it shown in Fig. 4. In this gate, A, B, C cells considered as the input, F cell as output with the following logical equation F(A,B,C)=A.B+A.C+B.C . Although this gate is the basic one in QCA technology, it is not a complete logical gate. To make a complete logical set, we need an inverter gate which is shown in Fig. 5. These two gates make a complete logical set by which every combinational logic circuit can be made. Various circuits have been designed by QCA technology [3][4][5]. But this technology suffers from two basic problems:

1- High construction error which is a result of excessive smallness of the cell in this technology (about 20 nm) and the inappropriateness of current methods of QCA constructions.
2- The errors and problems regarding timing and synchronizing different parts of QCA circuits.

The construction error will be solved as the technology develops or new methods such as self assemble are used. However, it is not a part of computer architecture. Here we focus on the system errors not physical ones.

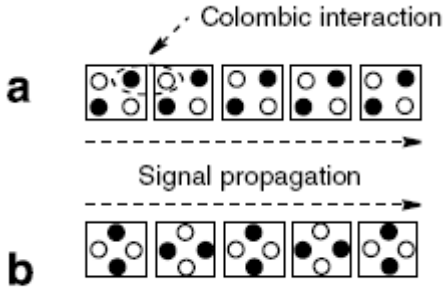

Fig. 3

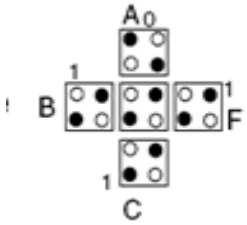

Fig. 4

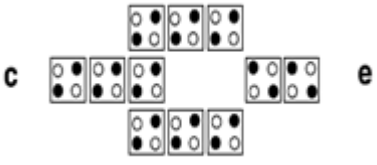

Fig. 5

3. Boolean Logic vs. NCL Logic

Boolean logic gives correct answers, but in practice when a series of input are applied to a continuously behaving Boolean combinational expression, before the stability of the circuit output(s) on correct ones, probably some invalid and unexpected output will appear(since some functions and signal paths are faster than others). A combinational Boolean logic expression cannot avoid this indeterminate behavior by itself, and even if these conditions could be avoided, there is still no means for a fixed evaluation of the result of the output based on the circuit's behavior.

Anyway, the output(s) of a combinational Boolean logic expression will be stable and finalized after a suitable and bounded time. Therefore after applying a new input set to a combinational Boolean logic expression it is necessary and sufficient to wait for a suitable time interval to be ensured that the output(s) is the correct resolution of the presented input set. Hence, in order to get the expected result of a logical design we need to attach a suitable time interval to the logical expression. Although measuring this period of time is not an easy task, it is possible and is currently used in designing synchronous logical circuits. Besides, an attempt has been made to remove the dependency of logical design on time which is generally known as asynchronous designing. C-elements and dual-rail methods are some of these proposed methods. Although these methods are one step forward, they are not applicable in general because of their complexity [6].

Attaching time to logical expression solve our main problem in logical designing. Nowadays this method is used in designing almost all logical circuits which are based on CMOS, but to use this method in designing QCA the main problem is the inherent difference of transferring signals in QCA in which the propagation delay is almost always more than the logical gate delay. Because routing and laying out of different parts of the circuit are different from its logical designing we can use some methods to design applicable circuits in QCA:

1- Doing routing and laying out different parts of a circuit together with its logical designing.
2- Remove timing from designing process completely.

The first solution is impossible for large circuits. The second solution is also impossible because of the nature of QCA in which clocking and transferring necessary power to the circuit are not separable as in CMOS. Thus we must design logical circuit based on QCA technology asynchronously.

4. LSGA method, using feedback or not

The main question about asynchronous designing is how we can design a logical circuit based on Boolean algebra which doses not need timing. Maybe considering Boolean algebra as the basic of asynchronous designing is the biggest mistake. One of the solutions which have been proposed quiet recently is introducing a new logic, Null Convention Logic (NCL), and designing logical circuits based on this logic. In this designing, there is no need for timing considerations. Because, against Boolean logic, this logic is complete by itself and does not need an outside means, it will solve our problem so that we will be able to make circuits without timing considerations in an asynchronous way, which will solve a lot of problems relating to designing and making logical circuits.

As it was mentioned, in designing based on the QCA technology, it is impossible to remove clocking and design circuits which work asynchronously. Designing large circuits by entering routing and laying out into the logical designing is practically impossible, but there is a moderate solution which is designing the small parts of the circuit synchronously and connecting them together asynchronously. In this method, the problem of synchronizing different parts will be solved. Moreover, there will no need to remove clocking out of the designing completely. This method is known as the Locally Synchronous Globally Asynchronous (LSGA).

In order to design and build logical circuits we should design the necessary logical gates in the given logic. As it was discussed before, using Boolean logic in asynchronous designing is neither easy nor practical; therefore, the NCL logic is used in designing. So, necessary gates in the NCL logic should be designed by QCA technology. This is done in [7].

Another serious problem in designing circuits based on the QCA is the difficulty of build feedback paths. Lots of efforts have been done to solve this problem [8], but it is an inherent problem of the QCA technology.

Because of the difficulty of producing feedback, it's better to avoid using feedback in the QCA based circuits, especially in small domains. The problem that we may come across regarding designing by NCL logic is that in all designing, some gates with hysteresis characteristic are used. When these gates are designed using the QCA technology, they need inter gate feedback. Because of this reason, it is impossible or at least very difficult to build them practically.

As it was mentioned, although using the NCL logic and designing circuits using the LSGA method solve one of the most important problems in designing logical circuits based on the QCA technology, the inter gates feedback has been used in these method, which will produce further problems.

In the NCL logic there are three condition of true, false and lack of data (NULL), Instead of the two conditions of true or false as in traditional Boolean logic.

Two methods have been proposed to implement this logic:

1- Using the hysteresis property inside the gates.

2- Using a fourth condition as an intermediate one instead of using hysteresis property.

In order to solve the problem of the inter gate feedback and using the advantages of the LSGA designing, we use the second method. This method has not been considered in making gates based on CMOS [9]. The reason is that this method is more difficult and costs more than the first one. The main advantage of the second method here is that there is no need for the feedback in making the gates. Therefore, we use the advantages of designing in the form of LSGA as well as having no problem with the feedback inside the gates. Since there are 4 conditions in the second method and using the 4 conditions on a wire is a difficult and complex task (impossible in QCA), we use two wires with the following qualities:

Data, Data => encoded_Data

Data, Null => encoded_intermediate

Null, Data => encoded_intermediate

Null, Null => encoded_Null

Although there is a need for feedback in this design (between different parts of circuit), the feedback inside the gates, is not needed.

To design the gate in Fig. 6 we need two threshold gates, namely gate of threshold 1 and gate of threshold 4. The gate of threshold 1 is acts as logical OR gate and the gate of threshold 4 is act as logical AND gate. Each of these gates has 4 inputs.

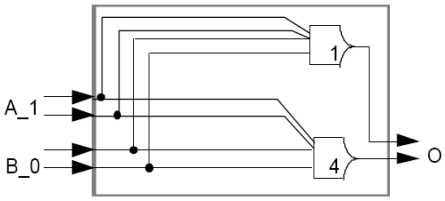

Fig. 6

The design of threshold 4 gate presented in Fig. 7 and design of threshold 1 gate presented in Fig. 8. Another characteristic of this design is the structural similarity of the two gates. They are different only in terms of polarity in two cells. The gate of threshold 1 has polarity 1 and that of threshold 4 has polarity -1. Fig. 9 shows the design of half adder in NCL logic. This circuit can be implemented by QCA technology provided the gates are replaced by the gates made above.

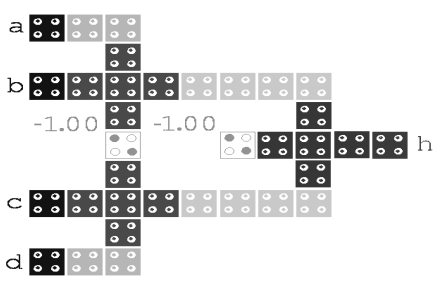

Fig. 7

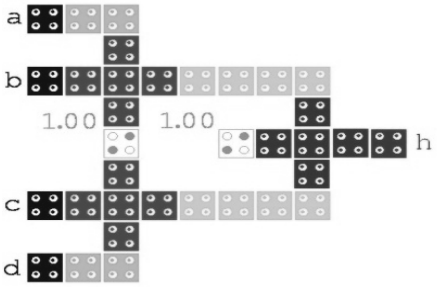

Fig. 8

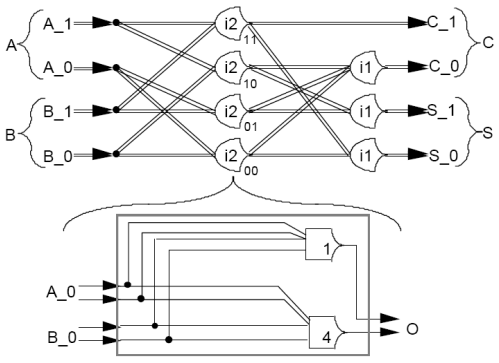

Fig. 9

5. CONCLUSION

This new LSGA method besides the advantage of LSGA design, (based on hysteresis property) didn't need to feedback inside the gates; it is one step forward to solve problems for build logical circuit based on QCA technology and use the advantage of this new technology. In this paper we tried to explain this new method.

6. References

[1] C.S. Lent, P.D. Tougaw, W. Porod, and G.H. Bernstein, "*Quantum cellular automata,*" Nanotechnology, vol.4, pp.49–57, 1993.

[2] C.S Lent and B. Isaksen, "*Clocked molecular quantum-dot cellular automata,*" IEEE Trans. Electronic Devices, vol. 50, no. 9, pp. 1890-1896, Sept. 2003

[3] W. Wang, K. Walus, and G.A. Jullien, "*Quantum-dot cellular automata adders,*" Proc. IEEE Nano 2003 Conf., San Francisco, CA,2003.

[4] A. Fijany, N. Toomarian, K. Modarress, and M. Spotnitz, "*Bit-serial adder based on quantum dots,*" NASA Technical Report, Jan. 2003.

[5] A. Vetteth, K.Walus, V.S. Dimitrov, and G.A. Jullien, "*Quantum-dot cellular automata carry-look-ahead adder and barrel shifter,*" Proc. IEEE Emerging Telecommunications Technologies Conf., Dallas, TX, Sept. 2002.

[6] K.M. Fant, "*Logically determined design clockless system design with NULL CONVENTION LOGIC,*" pp. 13-30, 2005.

[7] Minsu Choi and Nohpill Park, "*Locally Synchronous, Globally Asynchronous Design for Quantum-Dot Cellular Automata (LSGA QCA),*" IEEE International Conference on Nanotechnology, pp. 121-124, July 2005.

[8] M.T. Niemier and P.M. Kogge, "*Problems in designing with QCAs: layout=timing,*" Internatiomal journal of Circuit Theory and Applications, Vol.291(1), pp. 49-62, 2001.

[9] Yuan, J. S.; Kuang, W. "*Teaching Asynchronous Design in Digital Integrated Circuits,"* IEEE Transactions on Education, vol. 47, issue 3, pp. 397-404*,* Aug. 2004.