2011 2nd International Conference on Networking and Information Technology
IPCSIT vol.17 (2011) © (2011) IACSIT Press, Singapore

An Estimating SNR Method for IF Sampling Software Receiver

Li Shuangxun, Wang Zhan, Lou Shengqiang and Xin Qin

College of Electronic Science and Engineering, National Univ. of Defense Technology,
Changsha, Hunan Province, China
lishuangxun@nudt.edu.cn

Abstract. How to estimate the SNR of a SDR (Software-defined Radio) receiver system is discussed in this paper. Firstly, a basic estimating SNR method for a SDR receiver is presented by utilizing some existed theories. Secondly, the SNR effect from clock timing jitter to a SDR receiver is discussed, and the equations to calculate the clock timing jitter from clock phase noise is derived. Then, a new correct method is proposed for estimating the SNR of a SDR receiver. Finally, experiment result shows that the new method is more accuracy.

Keywords- IF Sampling, Software-Defined Radio, Timing Jitter, Phase Noise

1. Introduction

The SDR is a kind of software technique which can implement the hardware function of a radio communication system. Because of its flexible and opening application characteristics, the SDR has been one of the most important application techniques in the field of radar, sonar, electronic warfare and communication. How to select proper device and design a good performance SDR receiver is always a researching and discussing problem for SDR engineers. Therefore, it is very important to find a way to estimate the SNR of a SDR receiver system by utilizing the existed datasheets of the devices in a SDR receiver system so as to enhance work efficiency.

How to estimate the SNR of a designed SDR receiver system is discussed in this paper. First of all, a method to estimate the SNR of a SDR receiver is presented. Secondly, how to get the clock timing jitter from clock phase noise is discussed, and a correct method is proposed, which makes it more accuracy to estimate the SNR of a SDR receiver. Finally, the experiment result is presented.

2. The SNR of The SDR Receiver

Besides of large capacity memory and fast process speed, how much the noise introduced is an important performance standard to evaluate that whether a SDR system is designed advanced or not. In this section, we will discuss the SNR of a SDR system.

In a SDR system, in order to reduce analog processing steps, the intermediate frequency (IF) sampling is usually to be used. In order to guarantee the signal effective bandwidth, the high speed sampling AD device is needed. The noise introduced by the AD device would not be get ride of until the last signal processing step in the SDR system. Therefore, the AD noise is one of the main noise introduced to the system. The SNR effect of AD device to the system comes from four factors: ① the quantization noise to SNR; ② the ground-bound noise to the SNR; ③ the thermal noise to the SNR; ④ the aperture jitter to the SNR. If the selected AD is a kind of differential input device, the ground-bound noise introduced to the SDR system could be ignored, and the other three factors should be considered.

The quantization noise is one of the main factors which affect the SNR of ADC, and the quantization error would limit the dynamic range of ADC. If the quantization bits of an ADC is 8 and the quantization error belongs to uniform distribution, then the power of the quantization noise introduced to the ADC is

$$N_q = \Delta_{LSB}^2 / 12 \tag{1}$$

If the sampled signal is a single frequency full-scale range sine signal, the power of the quantization noise is

$$S_P = 2^{2N} \Delta_{LSB}^2 / 8 \tag{2}$$

Then the calculated SNR is

$$SNR_q = 10\lg\left(S_P / N_q\right) = 10\lg\left(\frac{3\times 2^{2N}}{2}\right) \tag{3}$$

For a high speed IF sampling system, the timing jitter of the sampling clock might make the sample time point deviate from its ideal sample time point, which would decrease the performance of the system and affect the SNR of the sampled data from ADC [1]. The clock timing jitter is consist of source clock timing jitter, clock driving device jitter and the aperture jitter of ADC itself. The aperture jitter of ADC can be found in the datasheet and the clock driving device jitter can be calculated by using the noise frequency multiplication formula. The source clock timing jitter is associated with the source clock phase noise. If the input analog signal to the ADC is a sine signal whose frequency and mean square root are f and σ_{jitter}. Then, as derived in [2], the SNR introduced by clock timing jitter is

$$SNR_j = -20\lg\left(2\pi f \sigma_{jitter}\right) \tag{4}$$

Therefore, the total SNR introduced by quantization, jitter and thermal noise is

$$SNR_{AD} = 10\lg\left(\frac{3\times 2^{2N}}{2+3\left(2^N \times 2\pi f \sigma_{jitter}\right)} - N_t\right) \tag{5}$$

where N_t is the power of the system thermal noise.

The output data rate from the ADC is the same as the ADC sampling frequency f_s. In the digital down conversion (DDC) process step, the digital data will be processed by digital filtering and data extract. Suppose that the final output signal bandwidth is B (B$<f_s$), then the input signal and $0.5f_s$ noise pass through the digital filter without amplitude changed, and the noise of B$\sim 0.5f_s$ bandwidth is eliminated by the DDC. So the SNR and the dynamic range is improved, which is

$$D_{improve} = 10\lg\left(f_s / 2B\right) \tag{6}$$

As mentioned above, from quantization noise, jitter noise, system thermal noise and DDC process gain, we can present the deserved SNR of a designed SDR system is

$$SNR_{system} = SNR_{AD} + D_{improve} \tag{7}$$

Take equation (5)(6) into equation (7), we can get the final SNR_{system} expression of a SDR system.

3. The Method to Calculate Clock Timing Jitter From Clock Phase Noise

From the above, we present a formula to estimate the SNR of a SDR receiver. The aperture jitter time is one of the main factors which affect the SNR of a SDR receiver. Therefore, how to get the clock timing jitter will be discussed in the section.

Nowadays, the method to acquire clock phase noise is convenient, but how to get the clock timing jitter is very difficult. Estimating the clock timing jitter from clock phase noise is the only indirectly way to get the clock timing jitter.

Because that the clock signal can be expanded by Fourier series, so the clock jitter characteristic is the same as the fundamental sine wave signal. Suppose there is a clock signal with phase noise. The clock frequency is f_0 , and the expression is

$$\begin{aligned} C(t) &= A\sin\left(2\pi f_0 t + \Delta\theta(t)\right) \\ &= A\sin\left(2\pi f_0\left(t + \frac{\Delta\theta(t)}{2\pi f_0}\right)\right) \end{aligned} \tag{8}$$

where $\Delta\theta(t)$ is the phase noise in the clock signal. Then the timing jitter can be presented as

$$\Delta t = \frac{\Delta\theta(t)}{2\pi f_0} \tag{9}$$

We can get timing jitter from the single side-band phase noise by the following steps. Firstly, we can get the phase noise power from the single side-band phase noise spectral density curve through the following equation

$$P_{noise} = \int_{f_L}^{f_H} S_\varphi(f)\,df = 2\int_{f_L}^{f_H} 10^{\frac{L(f)}{10}}\,df \tag{10}$$

Then we can calculate the mean square root of the phase jitter by the equation

$$\Delta\theta_{rms}(t) = \sqrt{P_{noise}} \tag{11}$$

Finally, we can get the mean square root of the timing jitter through the equation

$$\Delta t_{rms} = \frac{\Delta\theta_{rms}(t)}{2\pi f_0} \tag{12}$$

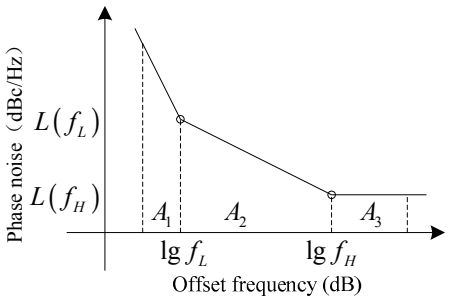

Figure 2. The curve of single side-band phase noise spectral density

The curve $L(f)$ of the single side-band spectral density is drawn by measured values, which has no analytical expression [3]. In view of the unique properties of the phase noise spectral density curve, the $L(f)$ is assumed to be consist of several linear functions in the engineering application [4], as showed in Fig. 1. Suppose that the slope of the single side-band spectral density $L(f)$ in area A_2 is

$$a = \frac{L(f)-L(f_L)}{\lg(f)-\lg(f_L)} = \frac{L(f_H)-L(f_L)}{\lg(f_H)-\lg(f_L)} \tag{13}$$

From equation (13), we can get the linear function expression is

$$L(f) = a\left(\lg(f)-\lg(f_L)\right)+L(f_L) \tag{14}$$

Take equation (14) into equation (10), we can have

$$\begin{aligned}
P_{noise} &= 2\int_{f_L}^{f_H} 10^{\frac{L(f)}{10}}\,df = 2\int_{f_L}^{f_H} 10^{\frac{a(\lg(f)-\lg(f_L))+L(f_L)}{10}}\,df \\
&= 2\times 10^{\frac{L(f_L)}{10}}\cdot\int_{f_L}^{f_H} 10^{\frac{a}{10}(\lg(f)-\lg(f_L))}\,df \\
&= 2\times 10^{\frac{L(f_L)}{10}}\cdot\int_{f_L}^{f_H} \left(f/f_L\right)^{\frac{a}{10}}df \\
&= 2\times 10^{\frac{L(f_L)}{10}}\cdot f_L^{-\frac{a}{10}}\cdot\int_{f_L}^{f_H} f^{\frac{a}{10}}df \\
&= \begin{cases} 2\times 10^{\frac{L(f_L)}{10}}\cdot f_L^{-\frac{a}{10}}\cdot\left(\frac{a}{10}+1\right)^{-1}\left(f_H^{\frac{a}{10}+1}-f_L^{\frac{a}{10}+1}\right), & a\neq -10 \\ 2\times 10^{\frac{L(f_L)}{10}}\cdot f_L\cdot\left(\ln(f_H)-\ln(f_L)\right), & a=-10 \end{cases} \\
&= \begin{cases} 2\times 10^{\frac{L(f_L)}{10}}\cdot f_L\cdot\frac{\left(f_H/f_L\right)^{a/10+1}-1}{a/10+1}, & a\neq -10 \\ 2\times 10^{\frac{L(f_L)}{10}}\cdot f_L\cdot\ln\left(f_H/f_L\right), & a=-10 \end{cases}
\end{aligned} \tag{15}$$

Then we can have another expression of equation (15) is

$$, \quad P_{noise} = 2 \times 10^{\frac{N_{integrate}^{(new)}}{10}} \tag{16}$$

where

$$N_{integrate}^{(new)} = \begin{cases} L(f_L) + 10\lg(f_L) \\ +10\lg\left[\dfrac{\left(\dfrac{f_H}{f_L}\right)^{\frac{a}{10}+1} - 1}{\cdot \dfrac{a}{10}+1}\right] & a \neq -10 \\ L(f_L) + 10\lg(f_L) \\ +10\lg\left(\ln(f_H / f_L)\right) & a = -10 \end{cases} \tag{17}$$

In conclusion, if we use the above equations in this section, we can get the clock timing jitter from the clock phase noise.

In order to get the integration of a linear function, we generally use the original method such as the trapezoidal rule to estimate the integration value. There is some integration error when using the original method. The error expression between the calculated integration value through the trapezoidal rule and the value calculated through equation (17) is

$$\begin{aligned} Error_{integrate} &= N_{integrate}^{(old)} - N_{integrate}^{(new)} \\ &= \begin{cases} \lg\left(\dfrac{\left(\dfrac{f_H}{f_L}\right)^{a/2}\left(\dfrac{f_H}{f_L}-1\right)^{10}}{\left(\dfrac{(f_H/f_L)^{\frac{a}{10}+1}-1}{a/10+1}\right)^{10}}\right) & a \neq -10 \\ \lg\left(\dfrac{\left(\dfrac{f_H}{f_L}\right)^{a/2}\left(\dfrac{f_H}{f_L}-1\right)^{10}}{\ln^{10}\left(\dfrac{f_H}{f_L}\right)}\right) & a = -10 \end{cases} \end{aligned} \tag{18}$$

If we select arbitrary values of f_L and f_H and the values meet the equation $f_H / f_L = 10$, then we can draw the error curve as showed in Fig. 2. From the error changing trend, we can find that the error is zero when $a = -20$, the error is becoming larger with the a value is becoming small when $a < -20$. So when $a \neq -20$, the estimating clock timing jitter method proposed in this paper is more accurate than the original one.

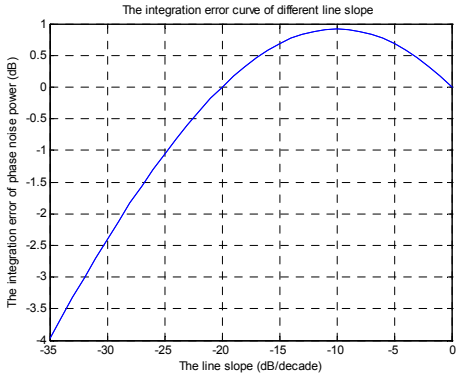

Figure 3. The integration error curve of the phase noise spectral density

4. The Experiment Result

In the section II, how to calculate the SNR of a designed SDR receiver is discussed, and a calculation formula is presented, which provides the theoretical basis to evaluate the performance of a SDR system. In this section, an experiment is presented to verify the proposed method of estimating SNR for a SDR system.

TABLE I. THE PARAMETER OF THE CLOCK PHASE NOISE

Offset Frequency(kHz)	The Single side-band Spectral Density (dBc)
0.001	-39
0.01	-75
1	-110
100	-147
1000	-150

In the system, the source clock selected is a kind of OCXO which is produced by SUN PEOPLE company. The frequency is 65.475MHz. The short term frequency stability is 1×10^{-9}. The phase noise characteristic is showed in Tab.1. Using the phase noise characteristic parameters and equation (16), we can calculate the mean square root of the source clock timing jitter, and the result is 24.0ps. If we use the trapezoidal rule and the same parameters to calculate the mean square root of the source clock timing jitter, the result is 17.8ps. The relative error is 26%, which is too big. Therefore, when we estimate the SNR of a SDR system, we should not use the trapezoidal rule all the time. Sometimes, we should use the more accurate method proposed in this paper.

In the experiment, we select AD6644 as the ADC device. The number of the AD6644 quantization bits is 14. The sampling rate is the clock frequency. The aperture jitter of AD6644 is 0.2ps [5], which can be ignored because of being too small compared to the source clock timing jitter. The GC5016 is selected as the DDC device [6]. The parameter settings of the GC5016 are: ①the local oscillation frequency is 15MHz; ② five stages CIC filter is set, and the decimation factor is 4; ③ two hundred and fifty five stages FIR filter is set, and the decimation factor is 4. The input analog signal to the AD device is a 16MHz sine wave, the amplitude peak to peak value is 100 mV. If ignoring the thermal noise, we can calculate the theoretical SNR of this system is 53.3dB by utilizing equation (7).

The Fig.3 shows the FFT result of the practical test data after AD and DDC. From the Fig.3, we can find the noise floor is about -93dB. Eliminating 16k FFT process gain [7], we can get the real SNR of the system is 53.9dB. The measured value is very close to the theoretical value (53.3dB), which verifies that the designed system meets the needs of design requirement.

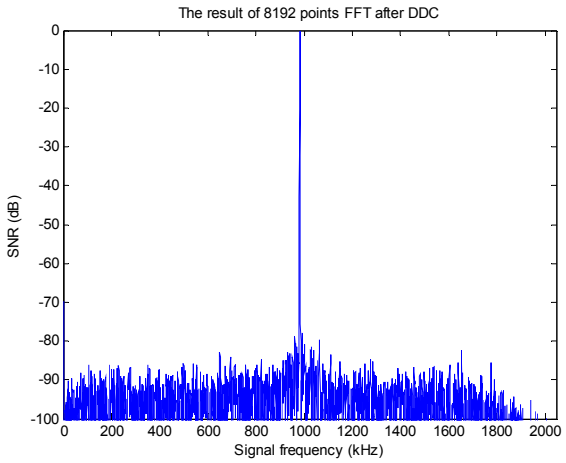

Figure 4. The result of 16k FFT

5. Conclusion

The SDR technique has become one of the most important application techniques in the field of radar, sonar, electronic warfare and communication, because of its flexible and opening application characteristics.

In this paper, a new estimating SNR method for SDR system is proposed. The practical test result shows that the new method is more accurate and more reliable than the original one in estimating SNR. The new method provides us important theoretical basis for designing a SDR receiver system.

6. References

[1] Sasikumar C., Abhijit C.. A High—Resolution Jitter Measurement Technique Using ADC Sampling[C]. Test Conference, 2001. Proceedings. Internationa1. 2001, 9, pp838—847

[2] Da Dalt, Nicola, et al (2002). On the Jitter Requirements of the Sampling Clock for Analogue-to-Digital Converters[J]. IEEE Trans Circuits and Systems - I, Sep 2002, vol.49(9), pp1354-1360..

[3] W. P. Robins. Phase noise in signal sources: (theory and applications) [M]. Peregrines on behalf of the IEE, 1982.

[4] Brannon. Brad. Sampled System and the Effects of Clock Phase Noise and Jitter. Applications Note AN-756[EB], Analog Devices. Inc, 2004

[5] Analog Devices. AD6644 datasheet[EB], http://www.analog.com, Analog Devices Inc, 2007

[6] Texas Instruments. GC5016 datasheet[EB], http://www.ti.com.cn, Texas Instruments Incorporated, 2007

[7] Walt Kester. Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor TUTORIAL MT003[EB], Analog Devices. Inc, 2009