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Design and Implementation of a Ternary FIR Filter using Sigma Delta Modulation

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Abstract. This paper describes the design and implementation of a single-bit FIR Filter with balanced ternary coefficients (i.e. -1/0/+1) aimed at general DSP applications. The fixed filter coefficients were computed using a sigma delta modulation technique. The filter is based on a hierarchical adder structure that can be pipelined for high performance that has been designed and simulated in VHDL. The filter structure exhibits low I/O and core area usage and high performance—achieving clock speeds in excess of 350MHz on a low-cost FPGA and over 600MHz on a high-performance device. The filter is intended to support video and audio processing applications in mobile communication systems.
Index Terms— Sigma Delta Modulation, FPGAs, Ternary FIR Filter, VHDL.

1. Introduction

Single-bit systems, in particular those based around Sigma-Delta modulation techniques, have been applied widely for the purpose of audio processing in systems such as mobile phones [1, 2, 5]. The attractive aspects of these single-bit systems are their intrinsic simplicity of operation, low power consumption, stability and efficient hardware implementation. More recently, technology scaling has allowed sigma delta modulation to operate above 10MHz and to achieve a dynamic range beyond the 70dB. This has made the technique applicable to mobile handset receivers and transmitters [5].

Applications of single-bit systems in mobile communications have tended to be restricted to the analog-to-digital conversion domain because it has proved difficult to perform complicated DSP tasks using 1-bit processing [6]. However in [1-4] a new generation of short word-length (SWL) systems (1 or 2 bits) were developed that can perform general-purpose DSP functions, including classical filtering and adaptive LMS filtering [3-4]. The key advantage of short word-length systems is that they do not require complex integer multiplication hardware [1, 3, 4], these being replaced by simple multiplexers. This is especially attractive for hardware implementation using Field Programmable Gate Arrays (FPGA), as reducing the number of general-purpose digital multipliers in the chip is a desirable goal. An FPGA design has the additional advantage that word lengths can be explicitly tailored to the requirements of the algorithm [8].

Balanced Ternary FIR Filters (TFF) operate with data and/or coefficient values of -1, 0 and +1. In this paper we extend the theoretical work of [1-4] and focus on the hardware implementation of TFF structures. We demonstrate the organization of an efficient Ternary FIR Filter mapped to an FPGA using a VHDL description. Our ultimate objective is the development of a number of small, fast filter modules targeting both video and audio applications in the mobile communication domain.

The remainder of this paper proceeds as follows. In section 2, the general design of the FIR filter with balanced ternary coefficients is discussed and an efficient implementation proposed based on a pipelined adder tree. Section 3 presents the design and simulation of the TFF, while in Section 4, we summarize and conclude the paper and point to future work.

2. The Ternary FIR Filter

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As shown in the general block diagram of 0, a FIR ternary filter comprises a tapped single-bit delay line followed by a coefficient multiplication stage and finally the addition of the partial products. The design of an effective FIR filter typically requires a very large number of coefficient taps (e.g., in excess of 1024 in [1]). In a short word length ternary filter, the tap coefficients will take the values of +1, 0 and -1, while the input data values, x(k), may either be single-bit (binary) or ternary, depending on the application. As a result, the multiplication stage will be reduced to a simple bit-wise AND/OR logic or a small look-up table (LUT). Thus it can be seen that is the parallel addition of the large number of partial products that forms the processing "bottleneck" in this architecture. This issue will be addressed in the following section.

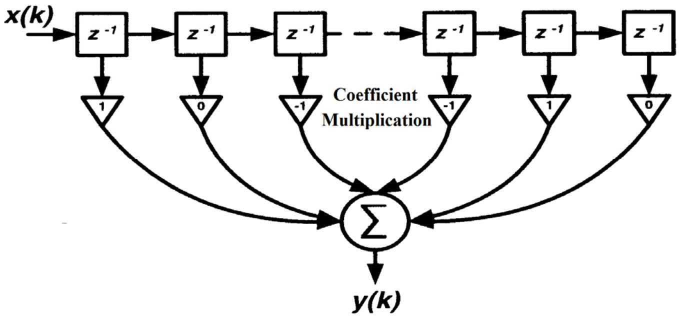

Fig. 1: Block Diagram of a Ternary FIR Filter (from [1]).

Mathematically the FIR filter output y(k) can be described by a convolution of the ternary taps h_i and the input signal x(k). If M is the order of the filter then the output of the filter is:

$$y(k) = \sum_{i=0}^{M} h_i x_{k-i} \quad \text{with } h_i \in \{1,0,-1\}. \tag{1}$$

In the implementation described here, the tap values (i.e. order of the filter M) have been generated via Sigma Delta modulation of the target impulse response. The process commences with a target low pass filter impulse response (0) that may be derived using any suitable design algorithm. We have used the Remez exchange method to derive the filter coefficients then interpolated before encoding to a ternary format (0) [1]. Various interpolation techniques are discussed in [10] along with their effect upon system frequency response. In this paper we have performed the interpolation using FFT method.

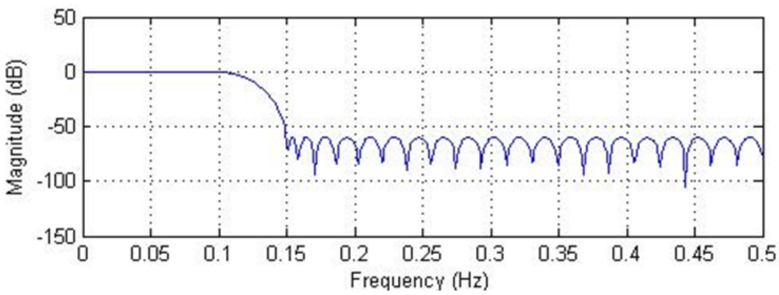

Fig.1: Normalized Target Impulse Response

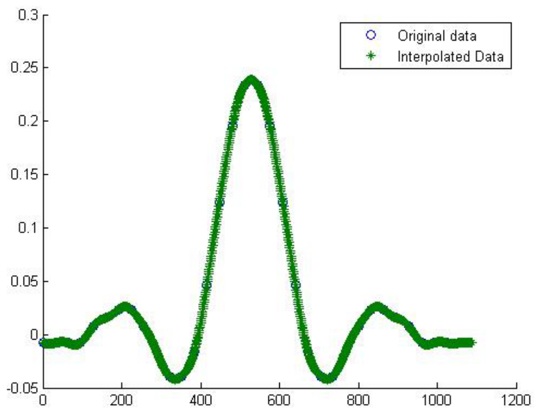

Fig.2: Interpolated Coefficients

The digital ΣΔM used to generate the ternary filter taps must have two properties. Firstly, the ternary quantizer is required to generate the tri-level output and, second, the ΣΔM should exhibit a flat signal frequency response over the desired bandwidth f_0 of the signal. A typical structure of a second order ΣΔM is shown in 0. The z-domain transfer function of this second order modulator is given by:

$$H(z) = G(z)z^{-1} + E(z)(1 - 2z^{-1} + z^{-2}) \tag{2}$$

where G (z) represents the target impulse response and E (z) represents the quantization noise transfer function. The noise shaping effect of the ΣΔM is evident from the presence of the filtering term, $(1 - 2z^{-1} + z^{-2})$ acting on the noise term, E(z). The frequency response of the above ΣΔM is given by [1]:

$$H_{\Sigma\Delta T}(e^{j\Omega}) = G(e^{j\Omega})e^{-j\Omega} + E(e^{j\Omega})(1 - 2e^{-j\Omega} + e^{-2j\Omega}) \tag{3}$$

where Ω =2π f/f_s is the normalized radian frequency.

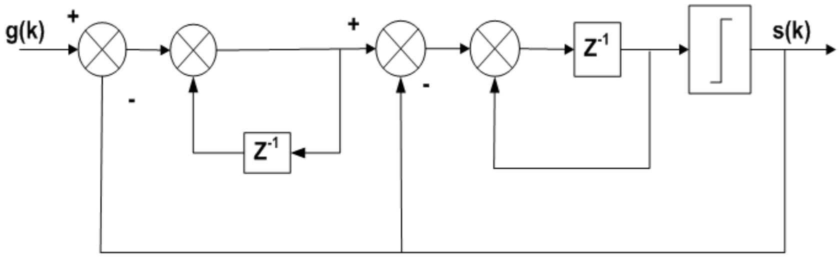

Fig.3: Block Diagram of a Second-order ΣΔ Modulator.

The ternary filter design assumes that the input signal is ΣΔM modulated with values of +1/-1 and that it operates at a specific OSR (Oversampling Ratio). As noted above, the input might alternatively be ternary encoded (±1, 0) but this will not alter the filter operation. The Signal to Quantization Noise Ratio (SQNR) can be improved by increasing the OSR. For example, in a second order ΣΔM the SQNR can be improved by 15 dB with each doubling of the OSR [9]. For the filter explored here (with 1024 taps) we have used an OSR of 32. Clearly, the upper bound on the Nyquist rate for the filter is related to the OSR and the maximum achievable clock frequency (FMAX) for the implementation. For example, operating on a video signal with a 6MHz bandwidth and an OSR of 32 would mandate an FMAX in excess of 200MHz.

3. Hardware Design of Ternary FIR Filter

As identified in Section 2, the operation of a ternary FIR Filter (see Fig. 1) comprises two main stages—the multiplication of input data with coefficients design followed by the addition of the large number of partial products (e.g., N=1024). Our implementation divides this up into N coefficient “multiply” blocks (i.e., by ±1, 0) followed by an adder tree with log_2N levels to perform the summation. We use a two-bit, two’s-complement representations for both the coefficients and the input data, which simplifies the arithmetic. Summing over N=1024 thus implies ten levels and the final multi-bit result is ±N. Because the two’s-complement representation is offset around zero, 12 bits are required to completely express the full output range of ±1024. As mentioned above a key advantage of SWL systems is that multiplication process becomes trivial—it can be performed using a small AND-OR logic equation instead of complex multiplication as in standard multi-bit processing. In the FPGA context, the multiplication of two 2-bit numbers will map to a small LUT element.

Many algorithms have been developed to reduce the latency as well as improve the efficiency of the circuit [6, 7]. In [7], a traditional Wallace adder tree is used as the tree structure for the implementation of adder and the VHDL code is generated by Matlab. In our work, we have focussed on techniques that map efficiently onto the FPGA organization. The general block diagram of the adder is given in Fig. 5. The adder tree comprises ten levels. At each stage of the tree, number of adder blocks halves while their length increases by one bit, culminating in a final 12-bit output. As a typical FPGA LUT structure takes a small number of inputs (in the range 6—8), the first two adder levels will be mapped to individual LUT blocks in the FPGA architecture that will operate in parallel. The remainder will comprise small ripple-carry blocks up to twelve bits long. Note that it would be equally possible to use optimised IP blocks created specifically for this purpose. In this paper, we have taken a more general approach, so that our results can be considered to be worse-case. In any case, we have tended to find only minimal performance difference between the short ripple-carry adder structures generated by this approach, and more complex techniques such carry-look ahead.

3.1. Simulation of Ternary FIR Filter

The filter design was created using VHDL and compiled, simulated and synthesized using Quartus-II 9.0 and Model Sim 5.8 targeting a small number of Altera™ Cyclone and Stratix FPGAs—chosen as representative of a range of FPGA components from low-cost to through to high performance. The design was explored using two different approaches, i.e. pipelined and non-pipelined. The non-pipelined version has a single 12-bit result resister at the output of the adder block (0) so that F_{MAX} is limited by the propagation delay of the 10-level adder block. The pipelined version places registers at the output of the multiplier and each stage of the adder tree so the primary limitation is the final 12-bit adder stage. The simulated results of both the designs with various FPGA devices are given in Table 1. Assuming an OSR of 32, it can be seen that we can easily process audio signals with any of the implementations, even the non-pipelined configurations. Processing a 6MHz video signal is also possible with most of pipelined implementations. The high performance Stratix IV device would be capable of supporting OSR values of up to 100, offering greatly improved filter performance in exchange for a significantly higher component cost and the larger power consumption implied by the increased operating frequency.

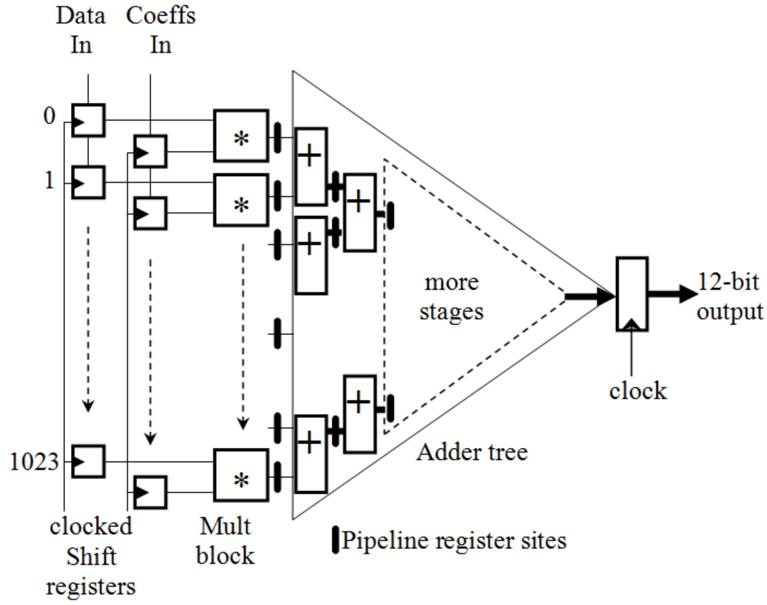

Fig. 4 General Structure of the TFF.

The pipelined version places registers at the sites shown—i.e., the output of the multiplier and between each stage of the adder tree.

4. Conclusion:

In this paper we have designed and simulated a Ternary FIR Filter that can be used for audio/and or video stream processing in mobile communication. A hierarchical pipelined adder structure has been described that is capable of operating speeds in excess of 300MHz using a low-cost FPGA. Using a high performance device (e.g., the 40nm Stratix IV) the filter can operate at more than 600MHz, easily supporting video data rates at an OSR of over 64. The filter operates on small 2's complement numbers and does not use any built-in specialised DSP components such as fast multipliers and thus occupies only a small part of the FPGA—for example, around 2% of the Stratix IV device.

Short Word Length systems offer a high performance and low-area solution to DSP systems with application in mobile communication systems as well as more general DSP disciplines such as biomedical, tele-monitoring and others. The current implementation uses a fixed coefficient set derived from the impulse response of the target filter. In future work we will expand this to encompass adaptive SWL systems, where the coefficients are derived from an analysis of the bit stream during operation.

Table 1. Mapping Results on Selected Altera FPGAs

Device	Configuration	Area (#elements)		F_{MAX} (MHz)
		Comb.	Registers	
Cyclone II EP2C15	Non-pipelined	3889	2060	56.8
	Pipelined	3766	5119	179.0
Cyclone III EP3C10	Non-pipelined	3889	2060	58.4
	Pipelined	3766	5119	209.8
Stratix II EP2S15	Non-pipelined	3138	2060	68.9
	Pipelined	3395	5119	251.3
Stratix III EP3SE50	Non-pipelined	3138	2060	90.8
	Pipelined	3395	5119	302.5
Stratix IV EP4SGX230DF	Non-pipelined	3135	2068	128.6
	Pipelined	3395	5119	617.7*

* internal clock rate; I/O pin limited to 400MHz

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